Enpirion® Power Datasheet

EN5322QI 2A PowerSoC Synchronous Buck DC-DC Converter with Integrated Inductor

General Description

The EN5322 is a high efficiency synchronous buck converter with integrated inductor, PWM controller, MOSFETS, and compensation providing the smallest possible solution size.

The 4 MHz operation allows for the use of tiny MLCC capacitors. It also enables a very wide control loop bandwidth providing excellent transient performance and reduced output impedance. The internal compensation is designed for unconditional stability across all operating conditions.

Three VID output voltage select pins provide seven pre-programmed output voltages along with an option for external resistor divider. Output voltage can be programmed on-the-fly to provide fast, dynamic voltage scaling with smooth transitions between VID programmed output voltages.

Applications

- Point of Load Regulation for Low Power Processors, Network Processors, DSPs' FPGAs and ASICs
- Replacement of LDOs
- Noise Sensitive Applications such as A/V and RF
- Computing, Computer Peripherals, Storage, Networking, and Instrumentation
- DSL, STB, DVR, DTV, and iPC

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5322QI	-40 to +85	24-pin QFN T&R
EVB-EN5322QI	QFN Evaluation Board	

Features

- **Revolutionary Integrated Inductor**
- **Total Solution Footprint as Small as 50 mm^2**
- 4 mm x 6 mm x 1.1 mm QFN Package
- 4 MHz Fixed Switching Frequency
- High Efficiency, up to 95 %
- Low Ripple Voltage; 8 mV_{P-P} Typical
- 2% Initial V_{OUT} Accuracy with VID Codes
- 2% Initial 0.6 V Feedback Voltage Accuracy
- 2.4 V to 5.5 V Input Voltage Range
- 2 A Continuous Output Current Capability
- Fast Transient Response
- Low Dropout Operation: 100 % Duty Cycle
- Power OK Signal with 5 mA Sink Capability
- Dynamic Voltage Scaling with VID Codes
- 17 µA Typical Shutdown Current
- Under Voltage Lockout, Over Current, Short Circuit, and Thermal Protection
- RoHS Compliant; MSL 3 260 °C Reflow

Application Circuit

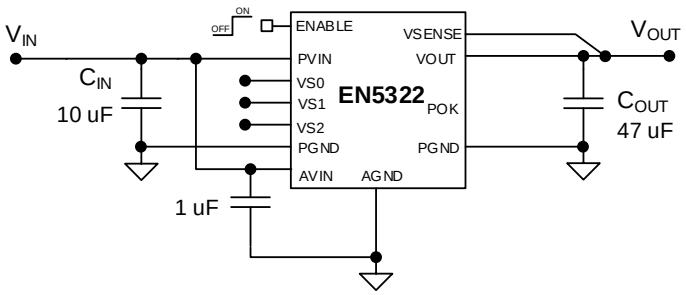


Figure 1. Typical Application Circuit

Absolute Maximum Ratings

CAUTION: Absolute maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Electrical Ratings	MIN	MAX
Voltages on: PVIN, AVIN, VOUT	-0.3 V	6.5 V
Voltages on: VSENSE, VS0, VS1, VS2, ENABLE, POK	-0.3 V	V_{IN}
Voltage on: VFB	-0.3 V	2.7 V
ESD Rating (Human Body Model)	2 kV	
ESD Rating (Charge Device Model)	500 V	
Absolute Maximum Thermal Ratings		
Ambient Operating Range	-40 °C	+85 °C
Storage Temperature Range	-65 °C	+150 °C
Reflow Peak Body Temperature MSL3 (10 s)		+260 °C

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Thermal Shutdown	T_{SD}		155		°C
Thermal Shutdown Hysteresis	T_{SDH}		15		°C
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}		6		°C/W
Thermal Resistance: Junction to Ambient (0 LFM)*	θ_{JA}		36		°C/W

* Based on a 2 oz. copper board and proper thermal design in line with JEDEC EIJ-JESD51 standards

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range	V_{OUT}	0.6	V_{IN} - $V_{DROPOUT}$	V
Output Current	I_{LOAD}	0	2	A
Operating Junction Temperature	T_J	-45	+125	°C

Note: $V_{DROPOUT}$ is defined as (I_{LOAD} x Dropout Resistance) including temperature effect.

Electrical Characteristics

V_{IN} = 5 V and T_A = 25 °C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lockout	V_{UVLO}	V_{IN} going low to high		2.2		V
UVLO Hysteresis				0.15		V
Output Voltage with VID Codes (Note 1)	V_{OUT}	T_A = 25 °C; V_{IN} = 5V I_{LOAD} = 100 mA VS2 VS1 VS0 VOUT (V) 0 0 0 3.3 0 0 1 2.5 0 1 0 1.8 0 1 1 1.5 1 0 0 1.25 1 0 1 1.2 1 1 0 0.8	 -2.0 -2.0 -2.0 -2.0 -2.0 -2.0 -2.0		 +2.0 +2.0 +2.0 +2.0 +2.0 +2.0 +2.0	%

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFB Voltage	V_{FB}	T_A = 25 °C; V_{IN} = 5V I_{LOAD} = 100 mA, VS0 = VS1 = VS2 = 1	0.588	0.600	0.612	V
Output Voltage with VID Codes (Note 1)	V_{OUT}	2.4 V ≤ V_{IN} ≤ 5.5 V, I_{LOAD} = 0 ~ 2 A, -40°C ≤ T_A ≤ +85°C VS2 VS1 VS0 VOUT (V) 0 0 0 3.3 0 0 1 2.5 0 1 0 1.8 0 1 1 1.5 1 0 0 1.25 1 0 1 1.2 1 1 0 0.8	 -3.0 -3.0 -3.0 -3.0 -3.0 -3.0 -3.5		 +3.0 +3.0 +3.0 +3.0 +3.0 +3.0 +3.0	%
VFB Voltage	V_{FB}	2.4 V ≤ V_{IN} ≤ 5.5 V, I_{LOAD} = 0 ~ 2 A, VS0 = VS1 = VS2 = 1, -40°C ≤ T_A ≤ +85°C	0.582	0.600	0.618	V
Dynamic Voltage Slew Rate		Switching between VID settings	0.975	1.5	2.025	V/ms
Soft Start Slew Rate		VID Mode VOUT Programming	0.975	1.5	2.025	V/ms
Soft Start Time		VFB Mode VOUT Programming	0.78	1.2	1.62	ms
VFB, ENABLE, VS0-VS2 Pin Input Current (Note 2)		-40°C ≤ T_A ≤ +85°C			+/-40	nA
ENABLE, VS0-VS2 Voltage Threshold		Logic Low Logic High	0.0 1.4		0.4 V_{IN}	V
POK Upper Threshold		V_{OUT} Rising		111		%
POK Upper Threshold		V_{OUT} Falling		102		%
POK Lower Threshold		V_{OUT} Rising		92		%
POK Lower Threshold		V_{OUT} Falling		90		%
POK Low Voltage		I_{SINK} = 5 mA, -40°C ≤ T_A ≤ +85°C		0.15	0.4	V
POK Pin V_{OH} Leakage Current		POK High, -40°C ≤ T_A ≤ +85°C			500	nA
Shutdown Current		ENABLE Low		17		µA
Quiescent Current		No Switching		800		µA
Quiescent Current		Switching, V_{OUT} = 1.2 V		15		mA
Current Limit Threshold		2.4 V ≤ V_{IN} ≤ 5.5 V, -40°C ≤ T_A ≤ +85°C	2.1	3.0		A
PFET On Resistance				160		mΩ
NFET On Resistance				60		mΩ
Dropout Resistance				200	300	mΩ
Operating Frequency	F_{OSC}			4		MHz
Output Ripple Voltage	V_{RIPPLE}	C_{OUT} = 1 x 47 µF 1206 X5R MLCC, V_{OUT} = 1.2 V, I_{LOAD} = 2 A		14		mV_{P-P}
		C_{OUT} = 2 x 22 µF 0805 X5R MLCC, V_{OUT} = 1.2 V, I_{LOAD} = 2 A		8		mV_{P-P}

Note 1: The tolerances hold true only if V_{IN} is greater than (V_{OUT} + $V_{DROPOUT}$).
Note 2: VFB, ENABLE, VS0-VS2 pin input current specification is guaranteed by design.

Pin Configuration

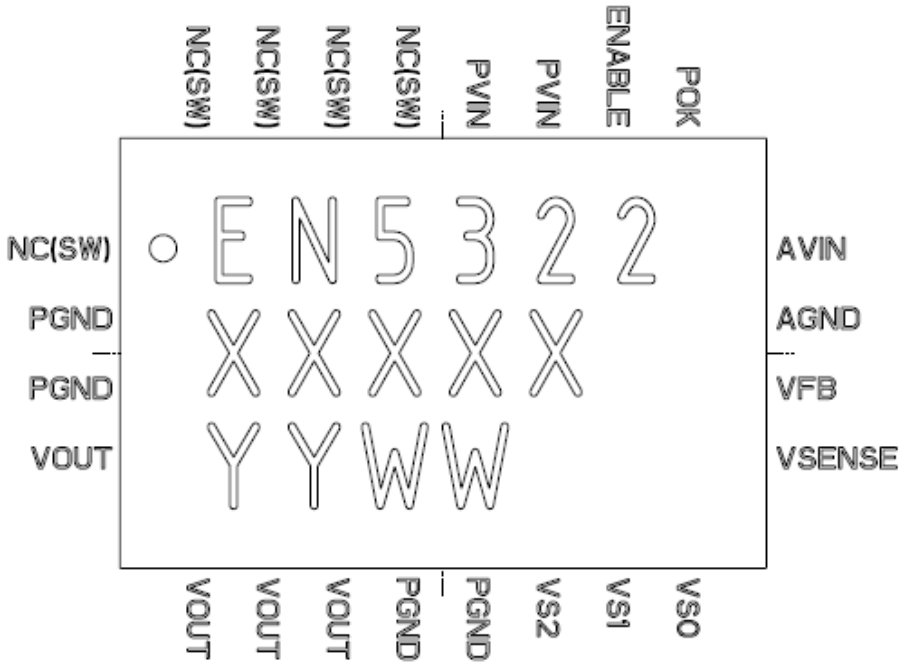


Figure 2. Pin Diagram, Top View.

Pin Description

PIN	NAME	FUNCTION
1, 21-24	NC(SW)	No Connect. These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
2-3, 8-9	PGND	Input/Output Power Ground. Connect these pins to the ground electrode of the input and output filter capacitors. Refer to Layout Considerations section for details.
4-7	VOUT	Voltage and Power Output. Connect these pins to output capacitor(s).
10-12	VS2-0	Output Voltage Select. These pins set one of seven preset output voltages and the external divider option (refer to Electrical Characteristics table for more details), and can be directly pulled up to V_{IN} or pulled down to GND; these pins must not be left floating.
13	VSENSE	Sense Pin for Internally Programmed Output Voltages with VID Codes. For either VID code or external resistor divider applications, connect this pin to the last local output filter capacitor for internal compensation.
14	VFB	Feedback Pin for External Voltage Divider Network. Connect a resistor divider to this pin to set the output voltage. Use 340 kΩ, 1% or better for the upper resistor.
15	AGND	Analog Ground for the Controller Circuits
16	AVIN	Analog Voltage Input for the Controller Circuits. Connect this pin to the input power supply. Use a 1 µF bypass capacitor on this pin.
17	POK	Power OK with an Open Drain Output. Refer to Power OK section.
18	ENABLE	Input Enable. A logic high signal on this pin enables the output and initiates a soft start. A logic low signal disables the output and discharges the output to GND. The ENABLE pin should not be left floating as it could be in an unknown and random state. It is recommended to enable the device after both PVIN and AVIN is in regulation. See ENABLE operation for details.

PIN	NAME	FUNCTION
19-20	PVIN	Input Power Supply. Connect to input supply. Decouple with input capacitor(s) to PGND.

Functional Block Diagram

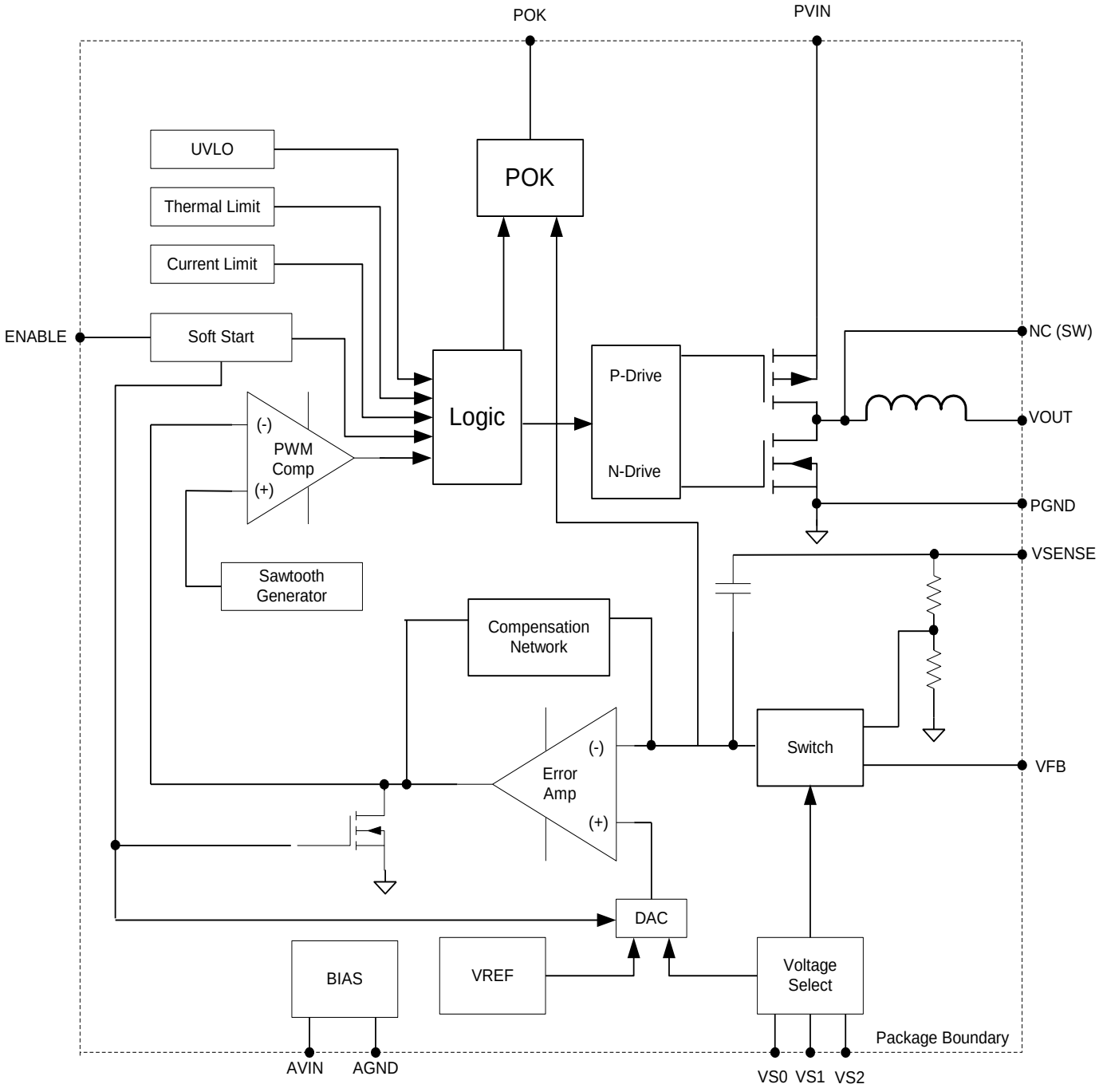
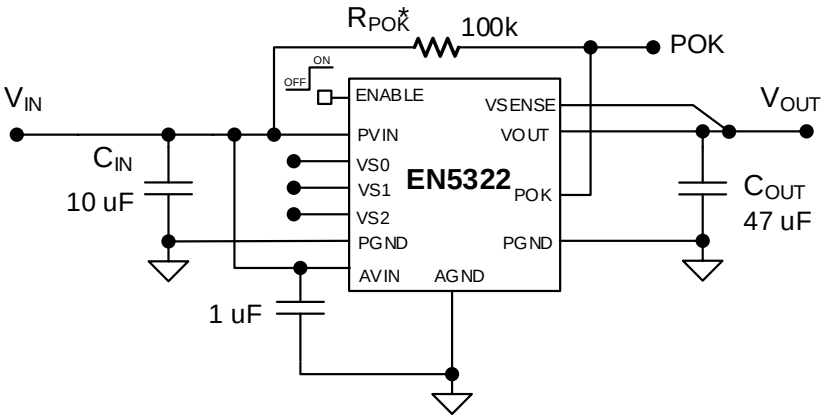


Figure 3. Functional Block Diagram.



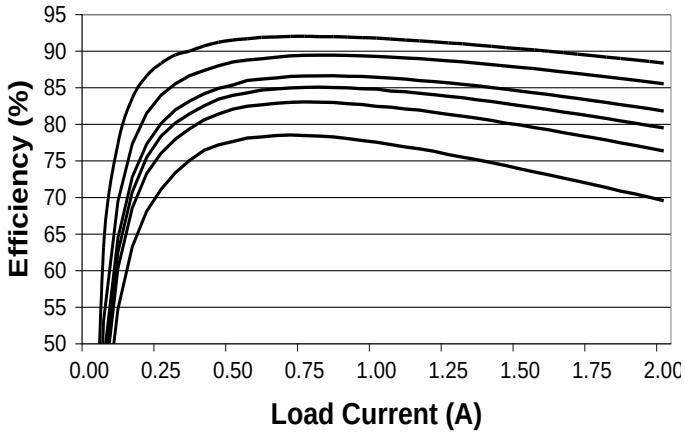
* Leave R_{POK} open if the POK function is not used.

Figure 4. Typical Application Circuit with VID Codes.
(*NOTE:* Enable can be separated from PVIN if the application requires it)

Typical Performance Characteristics

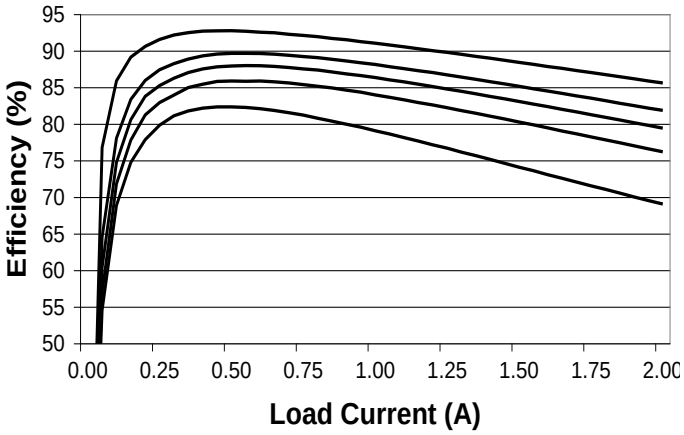
Circuit of Figure 4, V_{IN} = 5 V, V_{OUT} = 1.2 V and T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current (Vin = 5.0V)



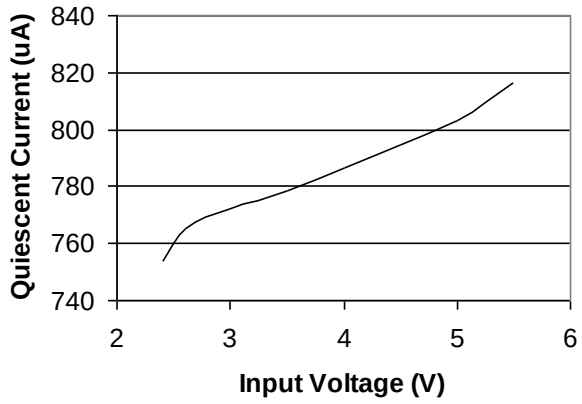
Top to Bottom: V_{OUT} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 0.8 V

Efficiency vs. Load Current (Vin = 3.3V)

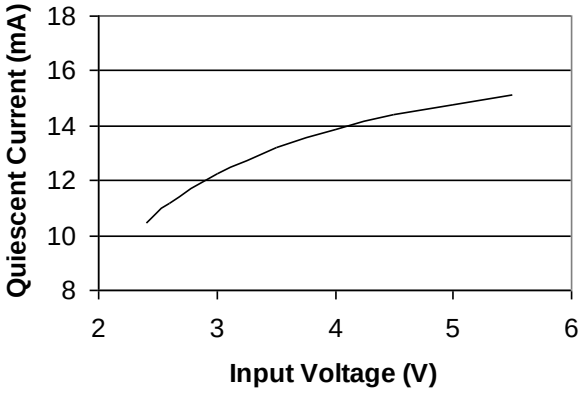


Top to Bottom: V_{OUT} = 2.5 V, 1.8 V, 1.5 V, 1.2 V, 0.8 V

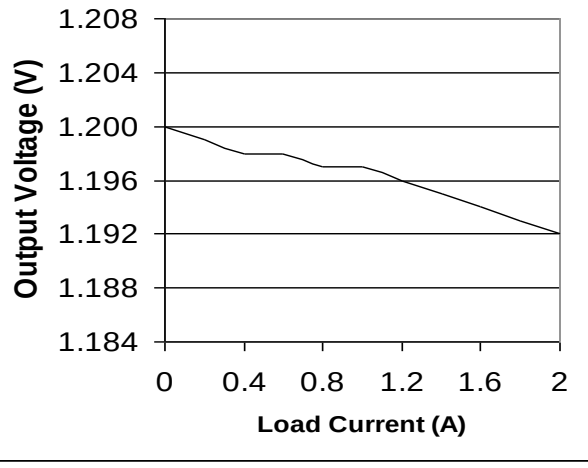
Quiescent Current (No Switching) vs. Input Voltage



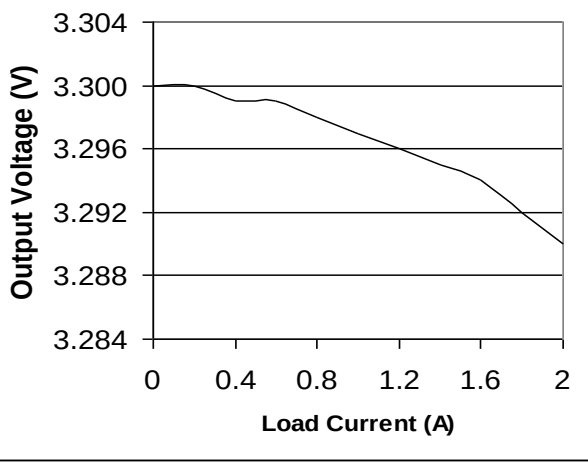
Quiescent Current (Switching) vs. Input Voltage



Load Regulation (Vin = 5 V)

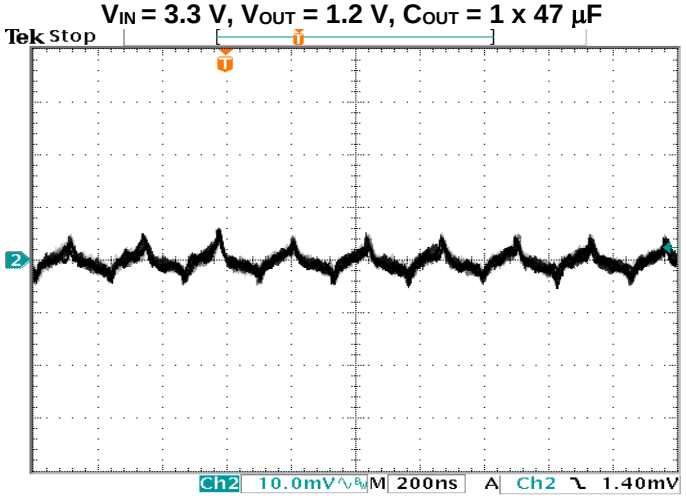


Load Regulation (Vin = 5 V)



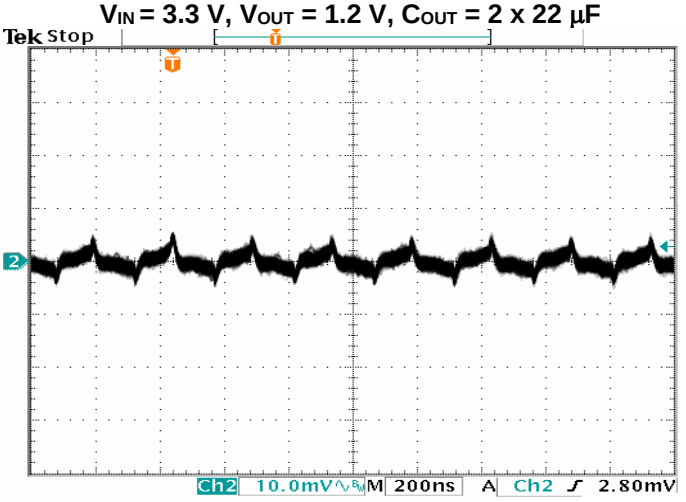
Output Ripple at 2 A Load (CH2: V_{OUT})

V_{IN} = 3.3 V, V_{OUT} = 1.2 V, C_{OUT} = 1 x 47 µF

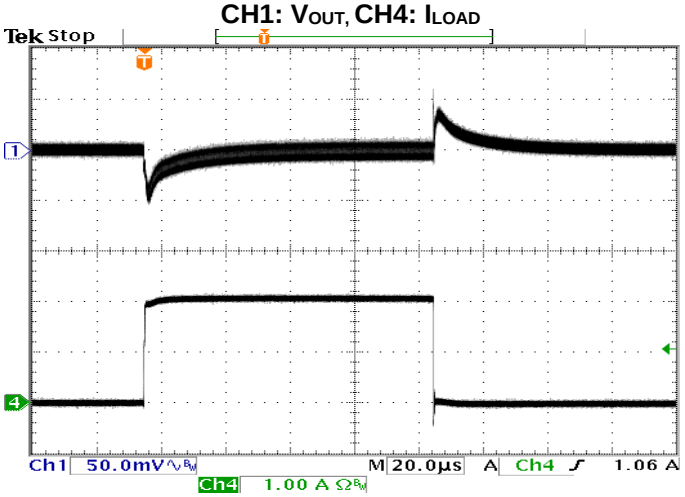


Output Ripple at 2 A Load (CH2: V_{OUT})

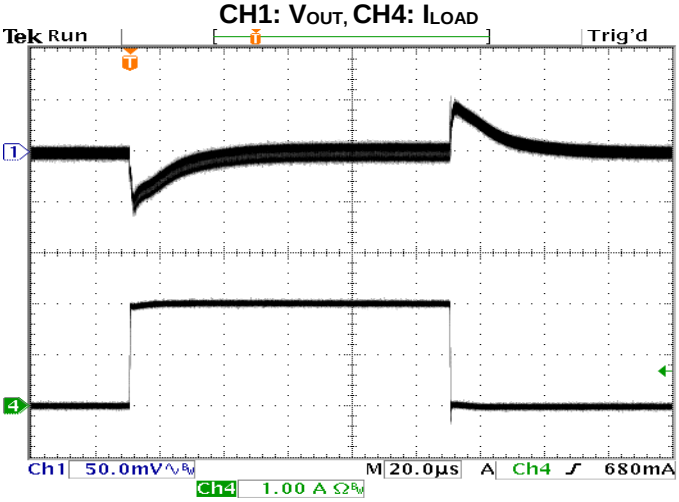
V_{IN} = 3.3 V, V_{OUT} = 1.2 V, C_{OUT} = 2 x 22 µF



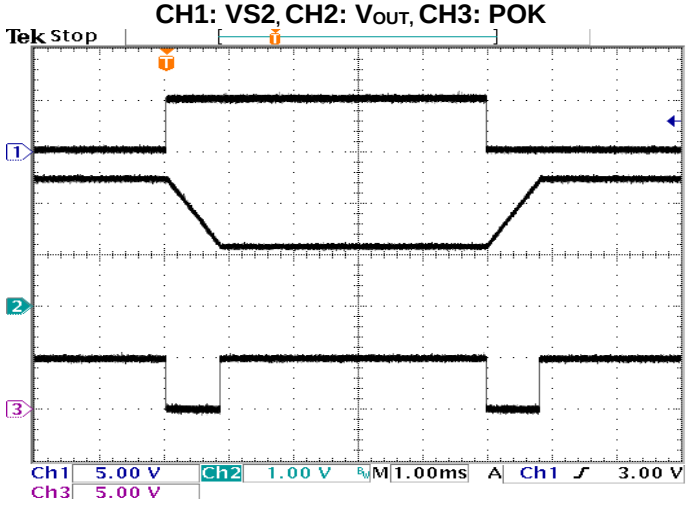
Transient Response at V_{IN} = 5 V
V_{OUT} = 1.2V, C_{OUT} = 1 x 47 µF
(0-2 A Load Step, slew rate ≥ 10A/uS)
CH1: V_{OUT}, CH4: I_{LOAD}



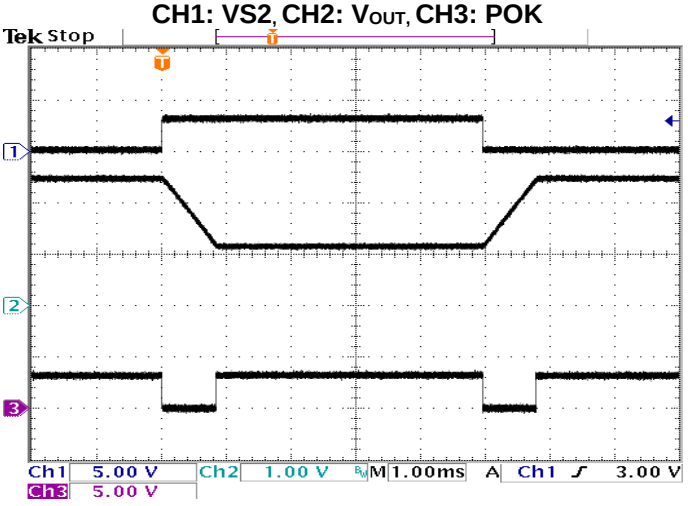
Transient Response at V_{IN} = 5 V
V_{OUT} = 3.3V, C_{OUT} = 1 x 47 µF
(0-2 A Load Step, slew rate ≥ 10A/uS)
CH1: V_{OUT}, CH4: I_{LOAD}



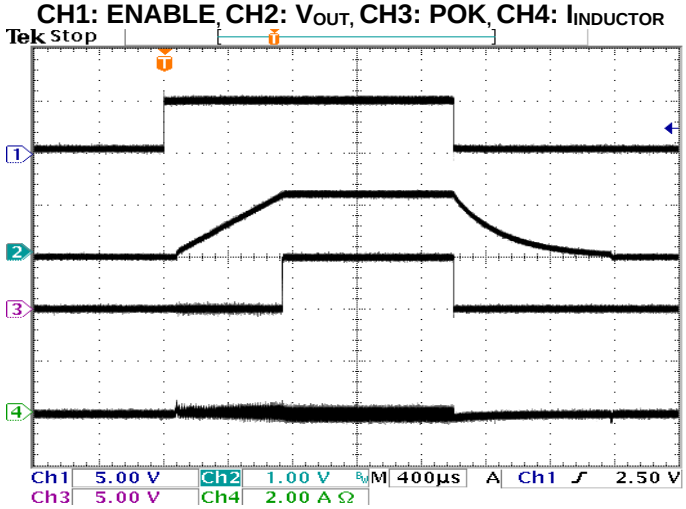
V_{OUT} Scaling with VID Codes at V_{IN} = 5 V
(V_{OUT} = 1.2 V – 2.5 V, I_{OUT} = 0 – 2 A)
CH1: VS2, CH2: V_{OUT}, CH3: POK



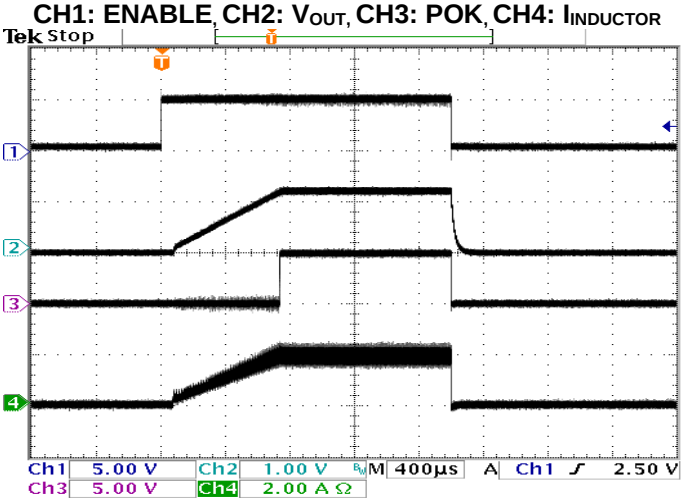
V_{OUT} Scaling with VID Codes at V_{IN} = 3.3 V
(V_{OUT} = 1.2 V – 2.5 V, I_{OUT} = 0 – 2 A)
CH1: VS2, CH2: V_{OUT}, CH3: POK



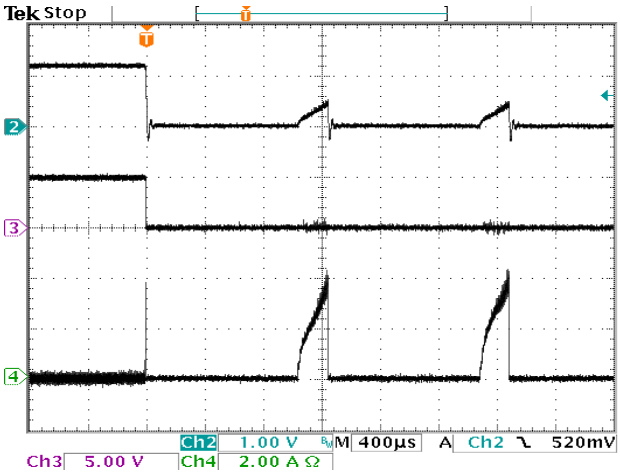
Power Up/Down at No Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH1: ENABLE, CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



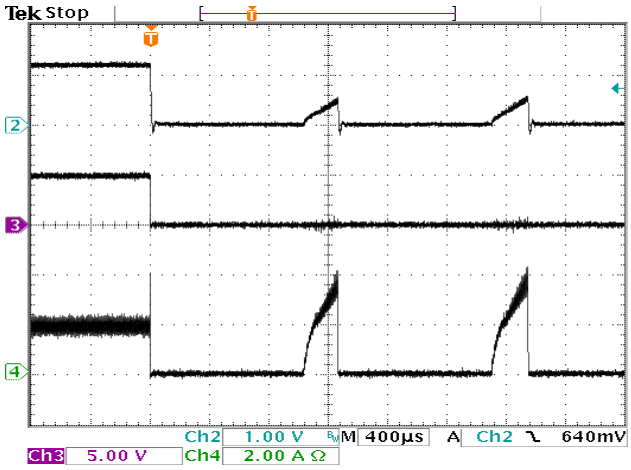
Power Up/Down at 0.6 Ω Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH1: ENABLE, CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



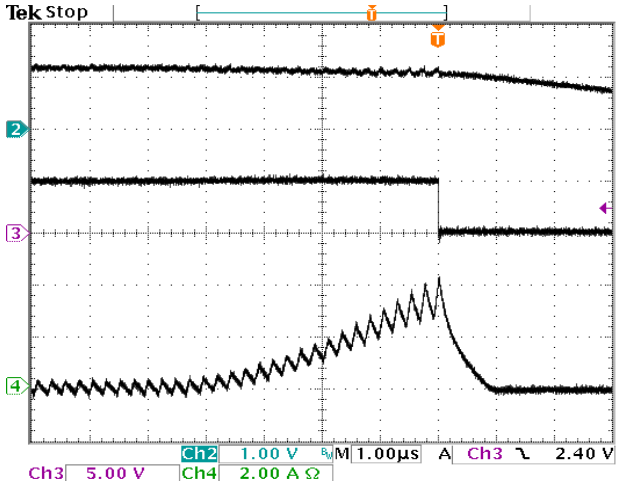
Output Over Load at No Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



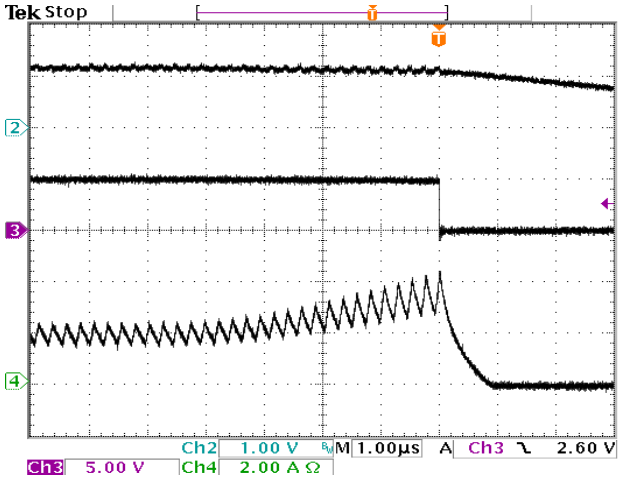
Output Over Load at 2 A Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



Output Over Load at No Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



Output Over Load at 2 A Load (V_{IN} = 5 V, V_{OUT} = 1.2 V)
CH2: V_{OUT}, CH3: POK, CH4: $I_{INDUCTOR}$



Functional Description

The EN5322 leverages advanced CMOS technology to provide high switching frequency, while also maintaining high efficiency.

Packaged in a 4 mm x 6 mm x 1.1 mm QFN, the EN5322 provides a high degree of flexibility in circuit design while maintaining a very small footprint. High switching frequency allows for the use of very small MLCC input and output filter capacitors.

The converter uses voltage mode control to provide high noise immunity, low output impedance and excellent load transient response. No external compensation components are needed for most applications.

Output voltage is chosen from one of seven preset values via a three-pin VID voltage select scheme. An external divider option enables the selection of any output voltage ≥ 0.6 V. The VID pins can be toggled dynamically to

implement glitch-free dynamic voltage scaling between any two VID preset values.

POK monitors the output voltage and signals if it is within ±10% of nominal. Protection features include under voltage lockout (UVLO), over current protection, short circuit protection, and thermal overload protection.

Stability over Wide Range of Operating Conditions

The EN5322 utilizes an internal compensation network and is designed to provide stable operation over a wide range of operating conditions. To improve transient performance or reduce output voltage ripple with dynamic loads you have the option to add supplementary capacitance to the output. When programming VOUT using the VID pins, the EN5322 is stable with up to 60 µF of output capacitance without compensation adjustment. Additional output capacitance above 60 µF can be accommodated with compensation adjustment depending on the application. When programming VOUT with the resistor divider option, the maximum output capacitance may be limited. Please refer to the section on soft start for more details. The high switching frequency allows for a wide control loop bandwidth.

Soft Start

The EN5322QI has an internal soft-start circuit that controls the ramp of the output voltage. The control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EN5322QI has two soft start operating modes. When VOUT is programmed using a preset voltage in VID mode, the device has a constant slew rate. When the EN5322QI is configured in external resistor divider mode, the device has a constant VOUT ramp time. Output voltage slew rate and ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup.

When operating in VID mode, the maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitance, at the load, is given as:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 1000uF$

When the EN5322QI output voltage is programmed using and external resistor divider the maximum total capacitance on the output is given as:

$C_{OUT\_TOTAL\_MAX} = 1.867x10^{-3}/V_{OUT}$ Farads

The above number and formula assume a no load condition at startup.

Over Current/Short Circuit Protection

When an over current condition occurs, V_{OUT} is pulled low. This condition is maintained for a period of 1.2 ms and then a normal soft start cycle is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

An under voltage lockout circuit will hold off switching during initial power up until the input voltage reaches sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between UVLO high and low states.

Enable

The ENABLE pin provides means to shut down the converter or initiate normal operation. A logic high will enable the converter to go through the soft start cycle and regulate the output voltage to the desired value. A logic low will allow the device to discharge the output and go into shutdown mode for minimal power consumption. When the output is discharged, an auxiliary NFET turns on and limits the

discharge current to 300 mA or below. In shutdown mode, the device typically drains 17μA. The ENABLE pin should not be left floating as it could be in an unknown and random state. It is recommended to enable the device after both PVIN and AVIN is in regulation. At extremely cold conditions below -30°C, the controller may not be properly powered if ENABLE is tied directly to AVIN during startup. It is recommended to use an external RC circuit to delay the ENABLE voltage rise so that the internal controller has time to startup into regulation (see circuit below). The RC circuit may be adjusted so that AVIN and PVIN are above UVLO before ENABLE is high. The startup time will be delayed by the extra time it takes for the capacitor voltage to reach the ENABLE threshold.

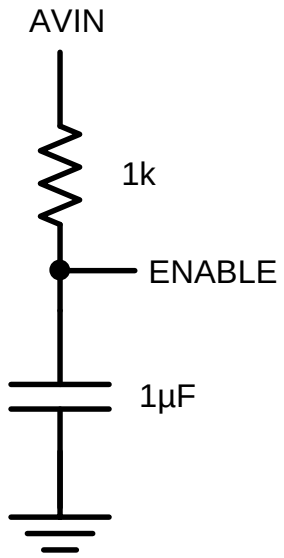


Figure 5: ENABLE Delay Circuit

Thermal Shutdown

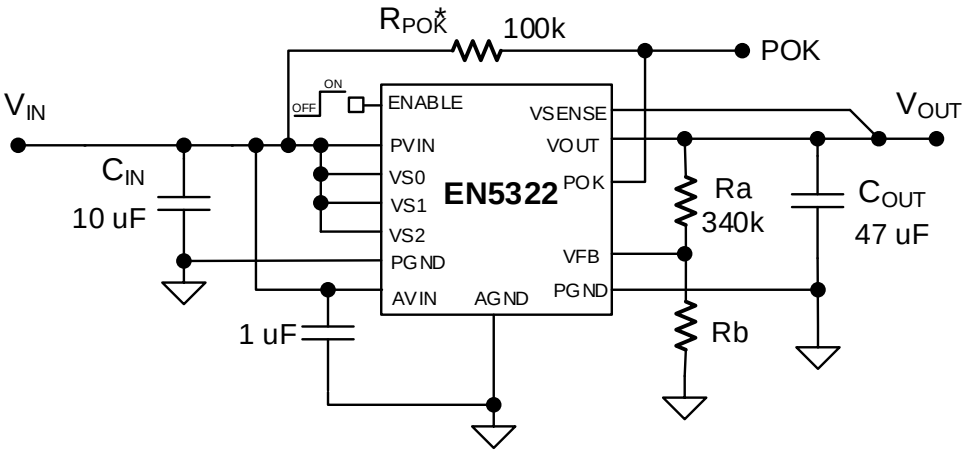
When excessive power is dissipated in the device, its junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature 155 °C, the thermal shutdown circuit turns off the converter, allowing the device to cool. When the junction temperature drops 15 °C, the device will be re-enabled and go through a normal startup process.

Power OK

The EN5322 provides an open drain output to indicate if the output voltage stays within 92% to 111% of the set value. Within this range, the POK output is allowed to be pulled high. Outside this range, POK remains low. However, during transitions such as power up, power down, and dynamic voltage scaling, the POK output will not change state until the transition is complete for enhanced noise immunity.

The POK has 5 mA sink capability for events where it needs to feed a digital controller with standard CMOS inputs. When POK is pulled high, the pin leakage current is as low as 500 nA maximum over temperature. This allows a large pull up resistor such as 100 kΩ to be used for minimal current consumption in shutdown mode.

The POK output can also be conveniently used as an ENABLE input of the next stage for power sequencing of multiple converters.



* Leave R_{POK} open if the POK function is not used.

Figure 6. Typical Application Circuit with External Resistor Divider.
(*NOTE:* Enable can be separated from PVIN if the application requires it)

Application Information

Setting the Output Voltage

To provide the highest degree of flexibility in choosing output voltage, the EN5322QI uses a 3 pin VID (Voltage ID) output voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Figure 4 shows a typical application circuit with VID codes. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

Table 1 shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. These pins must not be left floating.

Table 1. VID voltage select settings.

VS2	VS1	VS0	V_{OUT}
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	User Selectable

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to VIN or logic "high". The EN5322QI uses a separate feedback pin, V_{FB}, when using the external divider. VSENSE must be connected to V_{OUT} as indicated in Figure 6.

If the external voltage divider option is chosen, use 340 kΩ, 1% or better for the upper resistor

Ra. Then the value of the bottom resistor Rb in kΩ is given as:

$$Rb = \frac{204}{V_{OUT} - 0.6} k\Omega$$

Where V_{OUT} is the output voltage. Rb should also be a 1% or better resistor.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. It is recommended to follow the power-up and power-down sequencing to ensure that the EN5322QI is always sufficiently powered before the device begins operation.

Pre-Bias Start-up

The EN5322QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EN5322QI is not pre-biased when the EN5322QI is first enabled.

Input and Output Capacitor Selection

Low ESR MLC capacitors with X5R or X7R or equivalent dielectric should be used for input and output capacitors. Y5V or equivalent dielectrics lose too much capacitance with frequency, DC bias, and temperature. Therefore, they are not suitable for switch-mode DC-DC converter filtering, and must be avoided.

A 10 µF, 10 V, 0805 MLC capacitor is needed on PVIN for all applications. A 1 µF, 10 V, 0402 MLC capacitor on AVIN is needed for high frequency bypass to ensure clean chip supply for optimal performance.

A 47 µF, 6.3 V, 1206 MLC capacitor is recommended on the output for most applications. The output ripple can be reduced by approximately 50% by using 2 x 22 µF, 6.3V, 0805 MLC capacitors rather than 1 x 47 µF.

As described in the Soft Start section, there is a limitation on the maximum bulk capacitance that can be placed on the output of this device. Please refer to that section for more details.

Table 2. Recommended input and output capacitors

	Description	Mfg.	P/N
C_{IN}	10µF, 10V, X5R, 10%, 0805	Taiyo Yuden Murata Panasonic	LMK212BJ106KG GRM21BR71A106KE51L ECJ-2FB1A106K
C_{OUT}	47µF, 6.3V, X5R, 20%, 1206	Taiyo Yuden Murata Kemet	JMK316BJ476ML GRM31CR60J476ME19L C1206C476M9PACTU

POK Pull Up Resistor Selection

POK can be pulled up through a resistor to any voltage source as high as V_{IN}. The simplest way is to connect POK to the power input of the converter through a resistor. A 100 kΩ pull up resistor is typically recommended for most applications for minimal current drain from the voltage source and good noise immunity. POK can sink up to 5mA.

Layout Recommendations

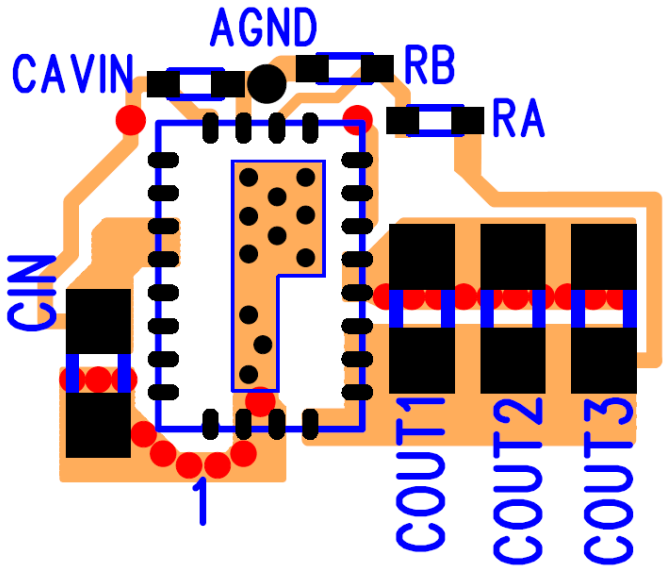


Figure 7. Optimized Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5322QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5322QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 3: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 7 this connection is made at the input capacitor. Connect a 1µF capacitor from the AVIN pin to AGND.

Recommendation 6: The layer 1 metal under the device must not be more than shown in Figure 7. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_A, R_B close to the VFB pin (See Figures 7). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 9: Altera provides schematic and layout reviews for all customer designs. Please contact local sales representatives for references to Power Applications Engineering support (www.altera.com/mysupport).

Design Considerations for Lead-Frame Based Modules

Exposed Metal Pads on Package Bottom

QFN lead-frame based package technology utilizes exposed metal pads on the bottom of the package that provide improved thermal dissipation and low package thermal resistance, smaller package footprint and thickness, large lead size and pitch, and excellent lead co-planarity. As the EN5322 package is a fully integrated module consisting of multiple internal devices, the lead-frame provides circuit interconnection and mechanical support of these devices resulting in multiple exposed metal pads on the package bottom.

Only the two large thermal pads and the perimeter leads are to be mechanically/electrically connected to the PCB through a SMT soldering process. All other exposed metal is to remain free of any interconnection to the PCB. Figure 8 shows the recommended PCB metal layout for the EN5322 package. A GND pad with a solder mask "bridge" to separate into two pads and 24 signal pads are to be used to match the metal on the package. The PCB should be clear of any other metal, including traces, vias, etc., under the package to avoid electrical shorting.

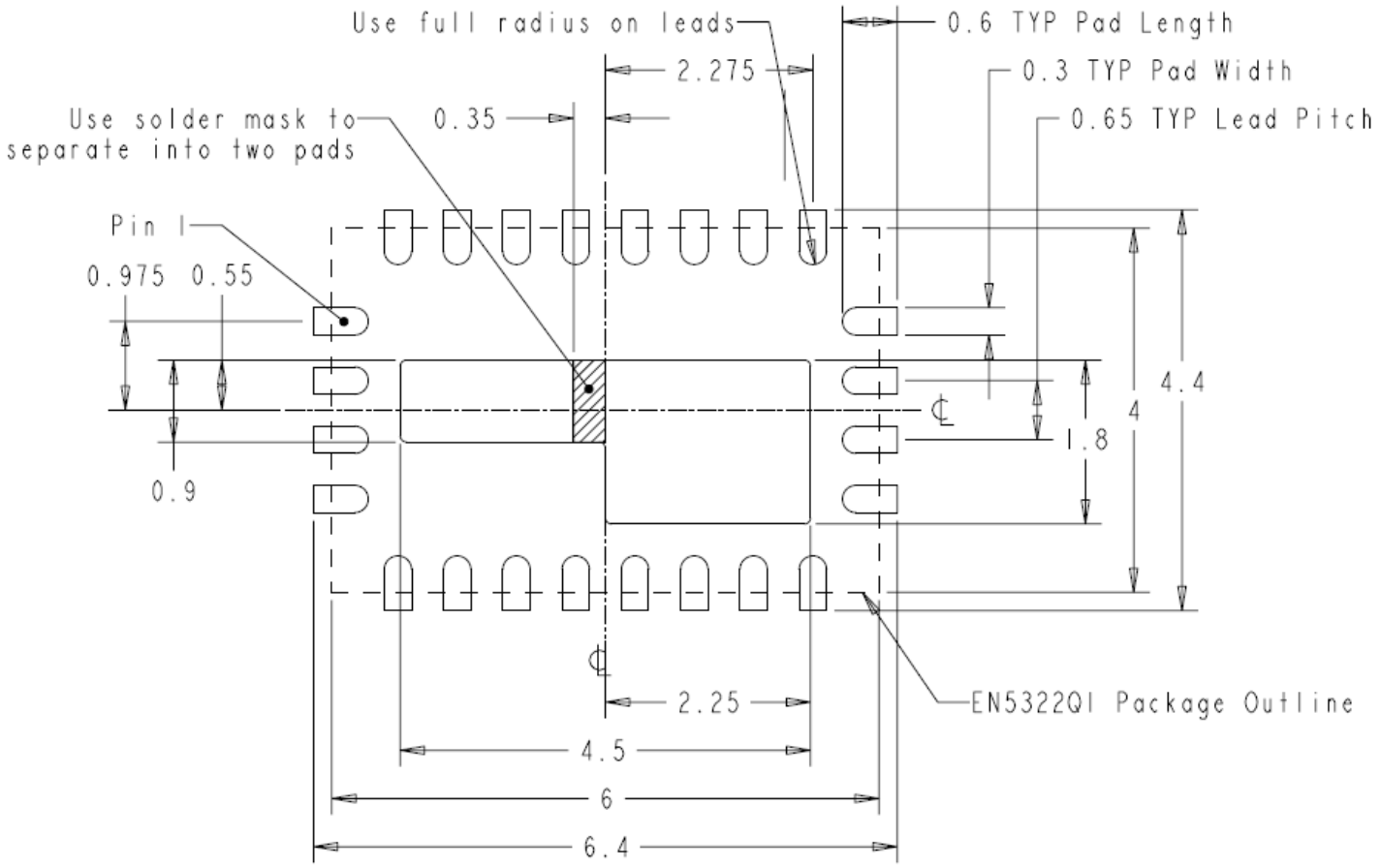


Figure 8. Recommended Footprint for PCB.

Package and Mechanical

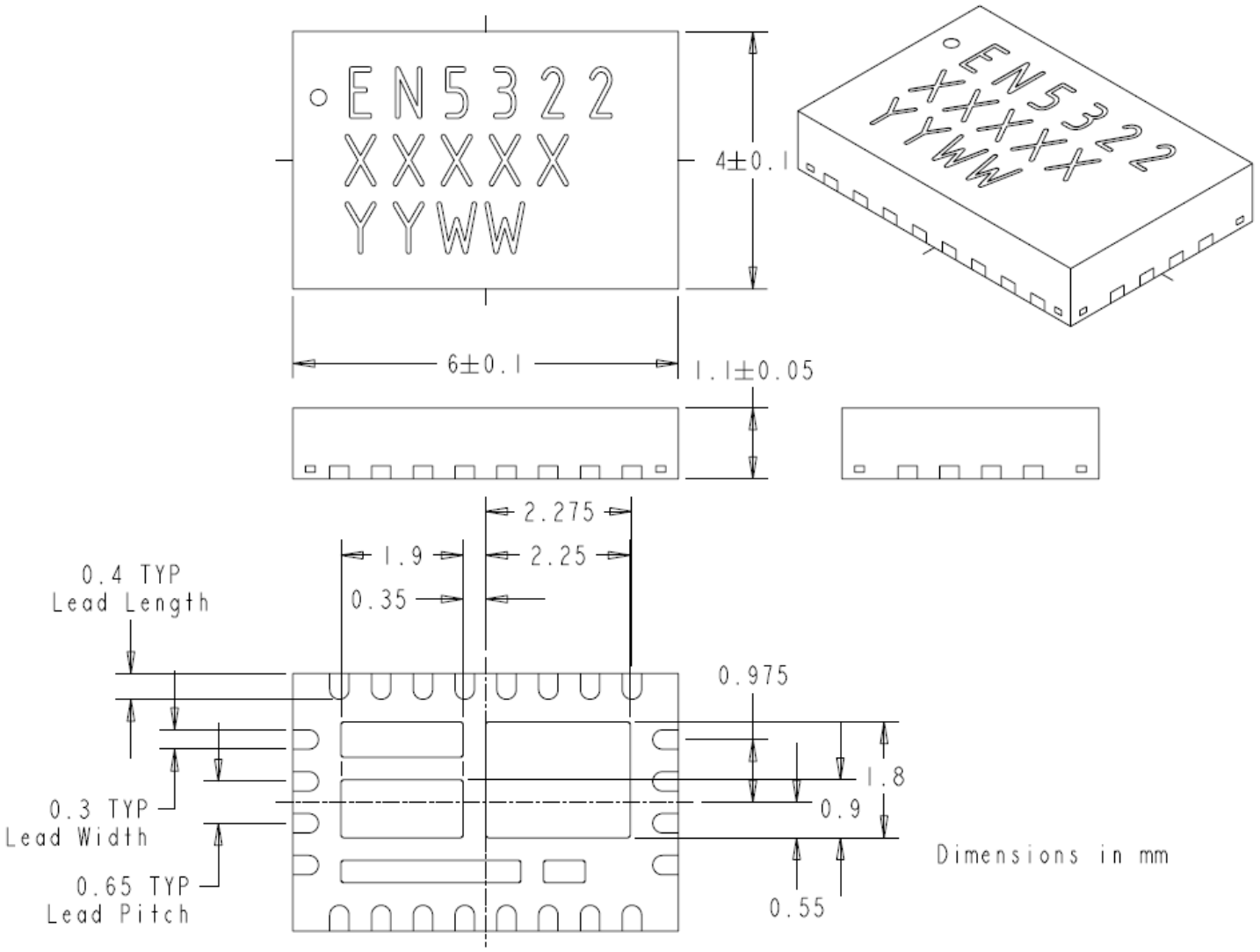


Figure 9. EN5322QI Package Dimensions

Revision History

Change(s) from Datasheet Rev F to Rev G in February 2014

- ENABLE functional description has been rewritten and updated to include delay circuit…… Page 11

Change(s) from Datasheet Rev G to Rev H in February 2014

- Updated Typical Application Circuits to show that ENABLE is best toggled after PVIN is stable…....Page 1
- Updated Power Up/Down Sequencing description……..……...……...Page 13

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