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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

January 2014

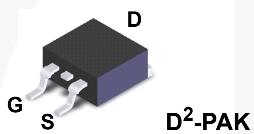
FDB13AN06A0

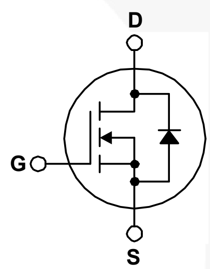
N-Channel PowerTrench® MOSFET
60 V, 62 A, 13.5 mΩ

Features
- $r_{DS(on)}$ = 11.5 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 62 A
- $Q_{g(tot)}$ = 22 nC (Typ.) @ V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

Formerly developmental type 82555

Applications
- Motor Load Control
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10V)	62	A
	Continuous (T_C = 100°C, V_{GS} = 10V)	44	A
	Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 43°C/W)	10.9	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	56	mJ
P_D	Power dissipation	115	W
	Derate above 25°C	0.77	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in² copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB13AN06A0	FDB13AN06A0	D^2-PAK	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 50V, V_{GS} = 0V, T_C = 150°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 62A, V_{GS} = 10V	-	0.0115	0.0135	Ω
		I_D = 31A, V_{GS} = 6V	-	0.022	0.034	Ω
		I_D = 62A, V_{GS} = 10V, T_J = 175°C	-	0.026	0.030	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	1350	-	pF
C_{OSS}	Output Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	260	-	pF
C_{RSS}	Reverse Transfer Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	90	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V; V_{DD} = 30V, I_D = 62A, I_g = 1.0mA		22	29	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V; V_{DD} = 30V, I_D = 62A, I_g = 1.0mA	-	2.6	3.4	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 30V, I_D = 62A, I_g = 1.0mA	-	8.5	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 30V, I_D = 62A, I_g = 1.0mA	-	5.9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 30V, I_D = 62A, I_g = 1.0mA	-	6.4	-	nC
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	-	158	ns
$t_{d(ON)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	9	-	ns
t_r	Rise Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	96	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	24	-	ns
t_f	Fall Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	26	-	ns
t_{OFF}	Turn-Off Time	V_{DD} = 30V, I_D = 62A, V_{GS} = 10V, R_{GS} = 12Ω	-	-	74	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 62A	-	-	1.25	V
		I_{SD} = 31A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 62A, dI_{SD}/dt = 100A/μs	-	-	25	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 62A, dI_{SD}/dt = 100A/μs	-	-	17	nC

Notes:
1: Starting T_J = 25°C, L = 45μH, I_{AS} = 50A.
2: Pulse width = 100s.

Typical Characteristics T_C = 25°C unless otherwise noted

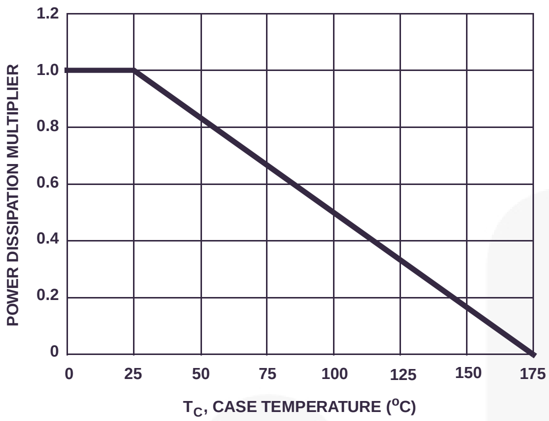


Figure 1. Normalized Power Dissipation vs Ambient Temperature

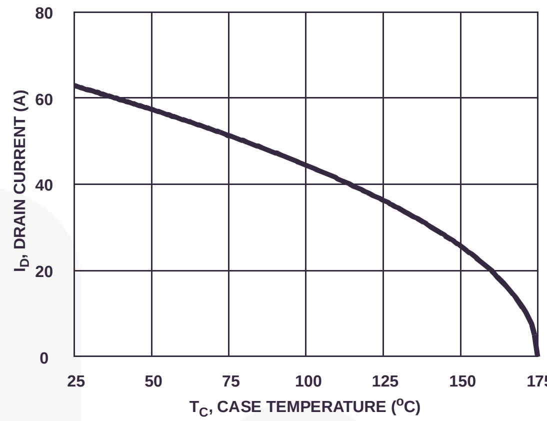


Figure 2. Maximum Continuous Drain Current vs Case Temperature

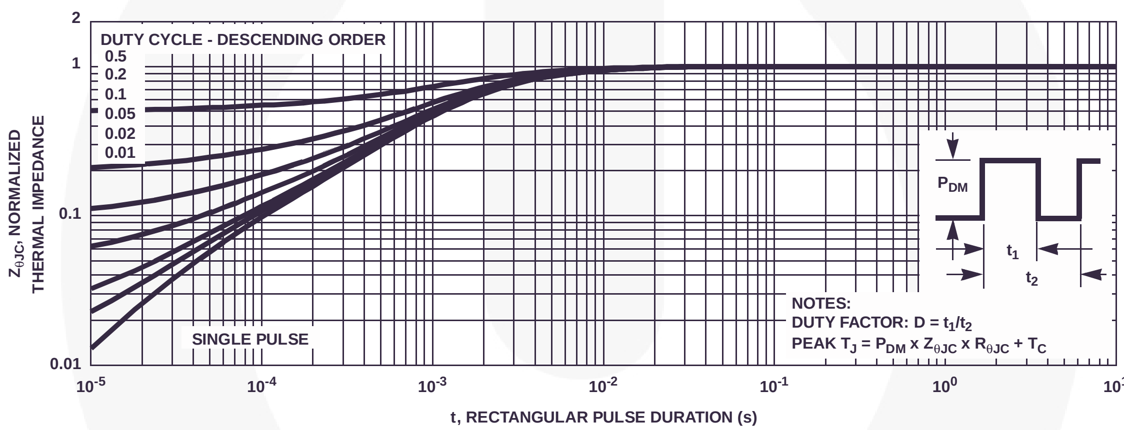


Figure 3. Normalized Maximum Transient Thermal Impedance

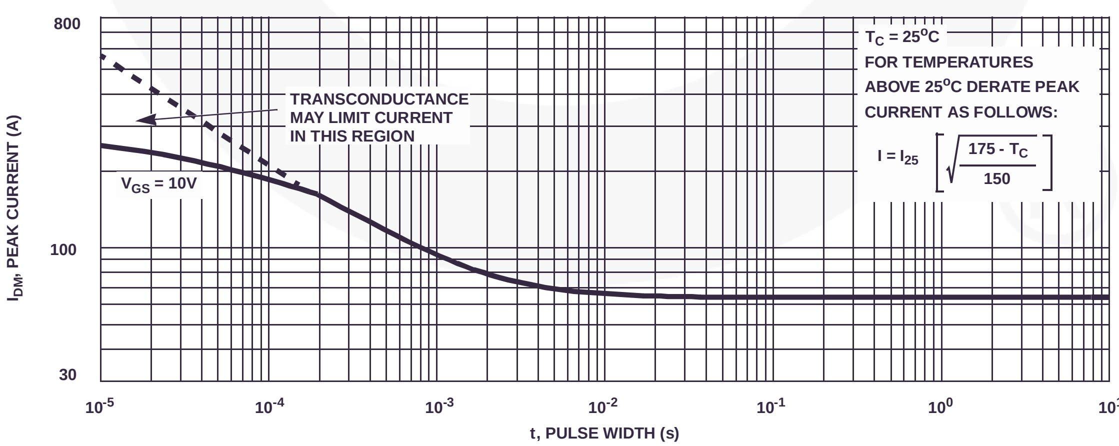


Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

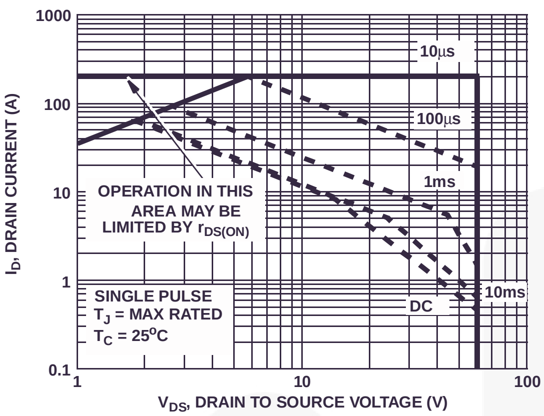
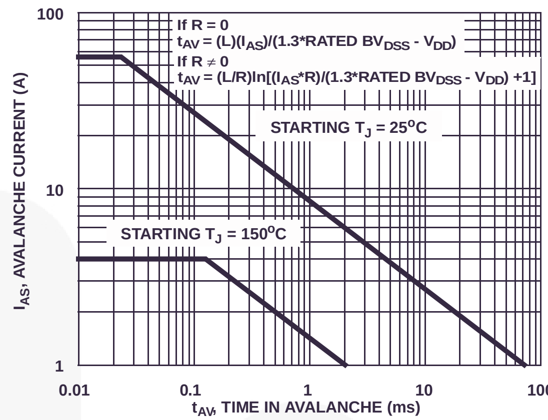


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

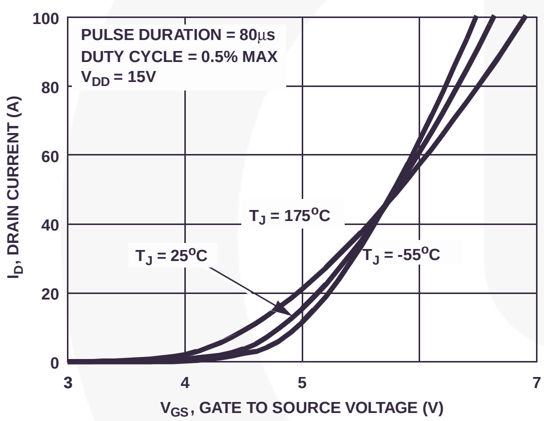


Figure 7. Transfer Characteristics

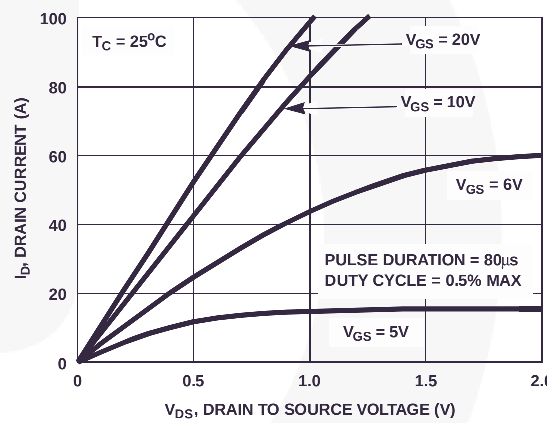


Figure 8. Saturation Characteristics

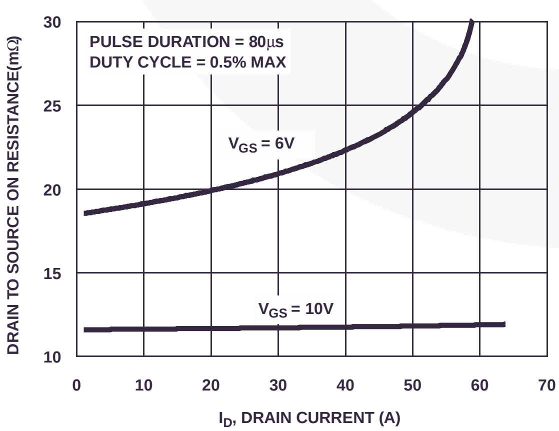


Figure 9. Drain to Source On Resistance vs Drain Current

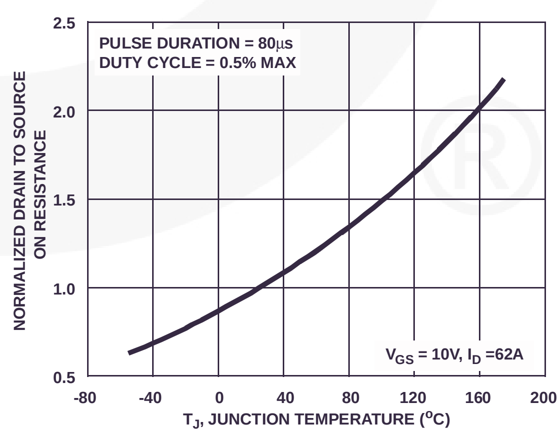


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics T_C = 25°C unless otherwise noted

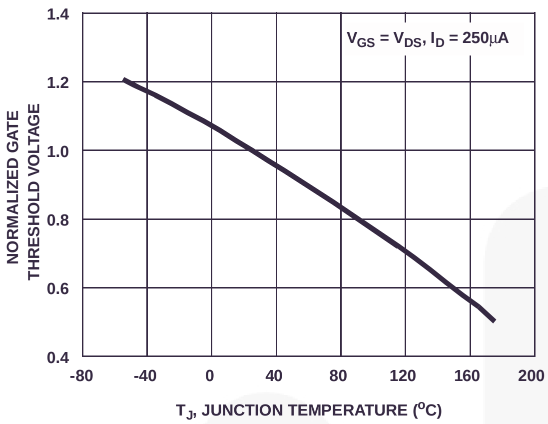


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

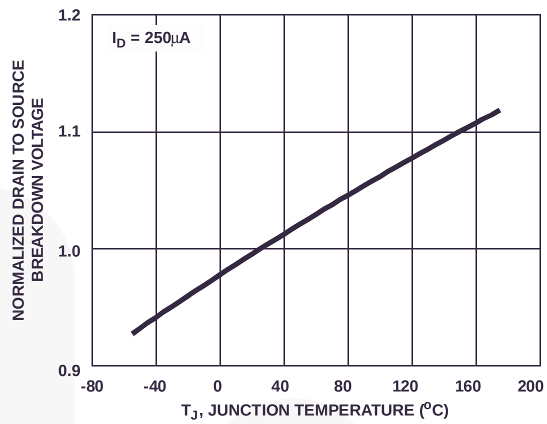


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

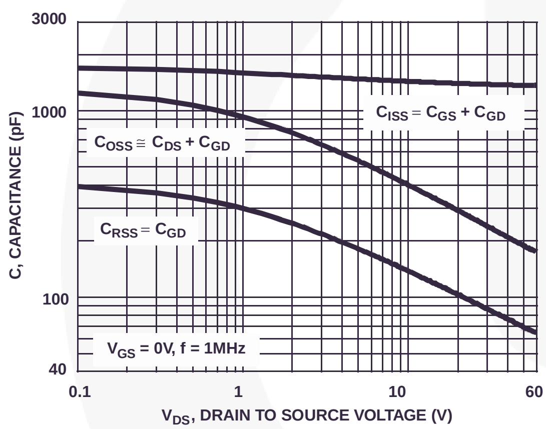


Figure 13. Capacitance vs Drain to Source Voltage

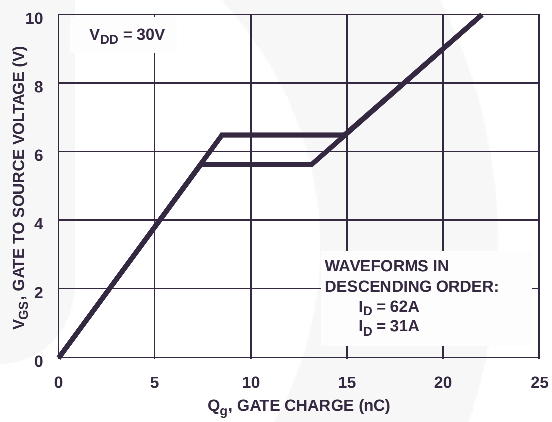


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

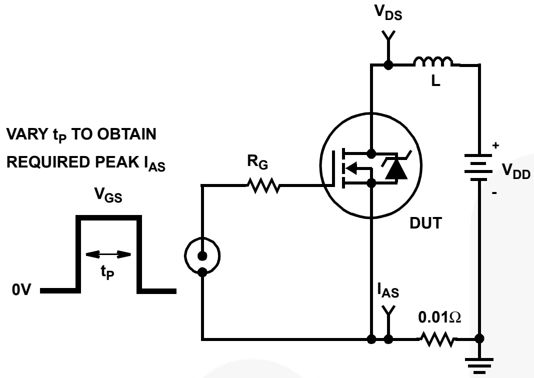


Figure 15. Unclamped Energy Test Circuit

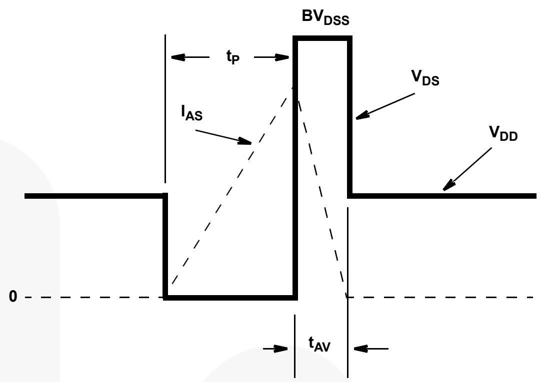


Figure 16. Unclamped Energy Waveforms

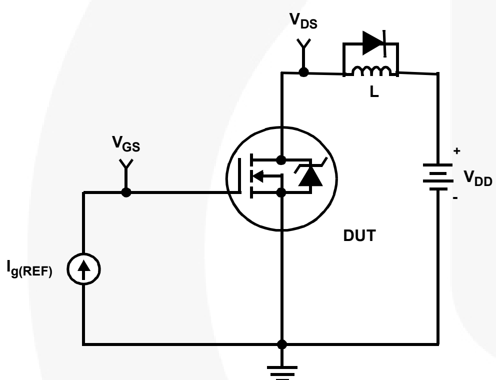


Figure 17. Gate Charge Test Circuit

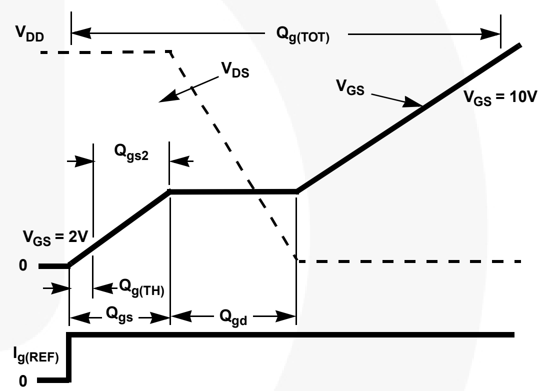


Figure 18. Gate Charge Waveforms

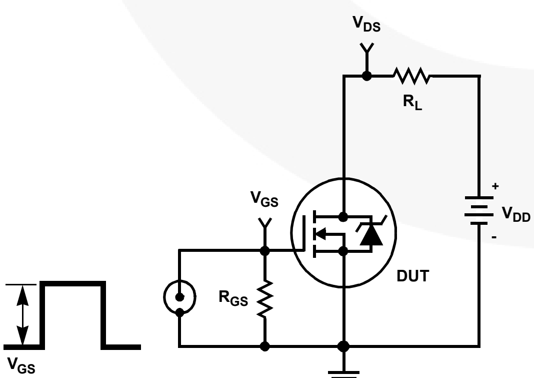


Figure 19. Switching Time Test Circuit

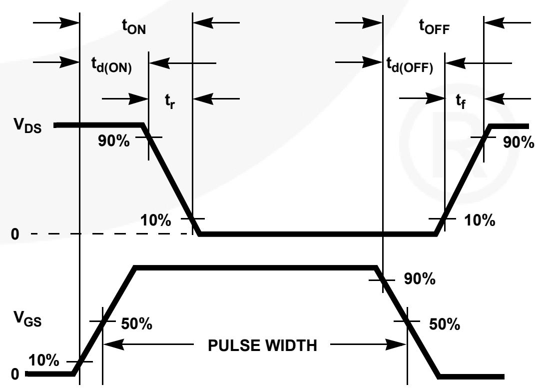


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \quad \text{(EQ. 3)}$$

Area in Centimeters Squared

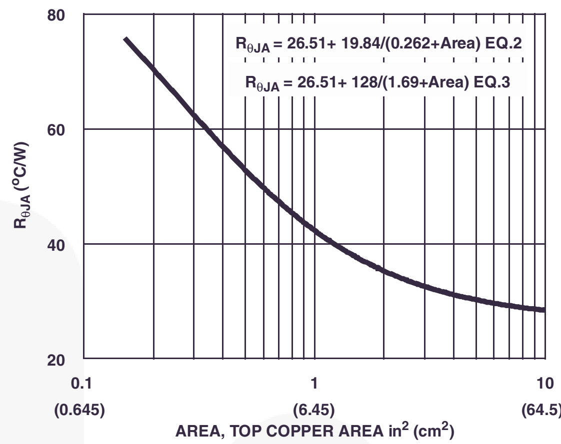
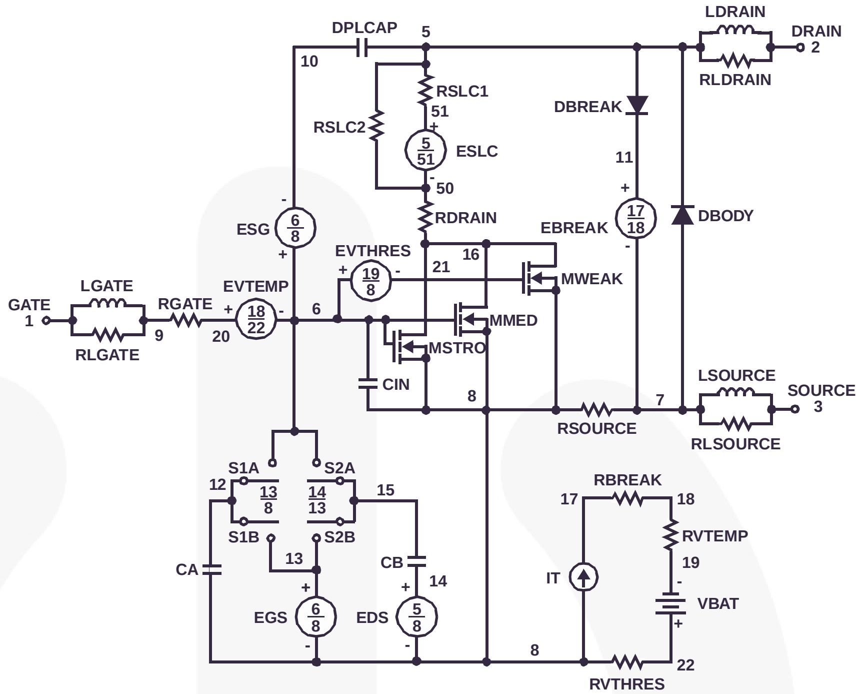


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model



.SUBCKT FDB13AN06A0 2 1 3 ; rev August 2002
Ca 12 8 5.1e-10
Cb 15 14 5.1e-10
Cin 6 8 1.3e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 65.40
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 6.9e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 2.91e-9

RLgate 1 9 69
RLdrain 2 5 10
RLsource 3 7 29.1

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 3.0e-3
Rgate 9 20 3.77
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 5.5e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*160),6))}

.MODEL DbodyMOD D (IS=1.5E-11 N=1.08 RS=3.3e-3 TRS1=2.2e-3 TRS2=2.5e-9
+ CJO=0.9e-9 M=5.1e-1 TT=1e-9 XTI=3.9)
.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=4.1e-10 IS=1e-30 N=10 M=0.45)

.MODEL MmedMOD NMOS (VTO=3.5 KP=6 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.77)
.MODEL MstroMOD NMOS (VTO=4.3 KP=50 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=2.88 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.77e+1 RS=0.1)

.MODEL RbreakMOD RES (TC1=9e-4 TC2=-5e-7)
.MODEL RdrainMOD RES (TC1=1.5e-2 TC2=4e-5)
.MODEL RSLCMOD RES (TC1=1.8e-3 TC2=1.7e-5)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.0e-5)
.MODEL RvtempMOD RES (TC1=-2.5e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5 VOFF=-2)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=0.5)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1.5)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

rev August 2002
template FDB13AN06A0 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=1.5e-11,nl=1.08,rs=3.3e-3,trs1=2.2e-3,trs2=2.5e-9,cjo=0.9e-9,m=5.1e-1,tt=1e-9,xti=3.9)
dp..model dbreakmod = (rs=1.5e-1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=4.1e-10,isl=10e-30,nl=10,m=0.45)
m..model mmedmod = (type=_n,vto=3.5,kp=6,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.3,kp=50,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.88,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-5,voff=-2)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-5)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1.5,voff=0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1.5)
c.ca n12 n8 = 5.1e-10
c.cb n15 n14 = 5.1e-10
c.cin n6 n8 = 1.3e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 65.40
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

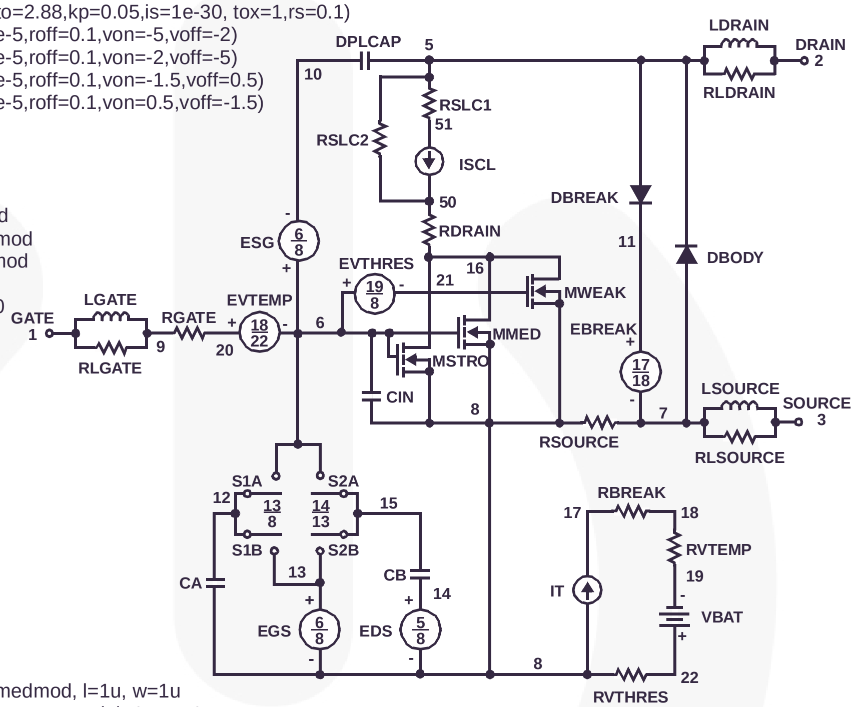
l.lgate n1 n9 = 6.9e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2.91e-9

res.rlgate n1 n9 = 69
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 29.1

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=9e-4,tc2=-5e-7
res.rdrain n50 n16 = 3.0e-3, tc1=1.5e-2,tc2=4e-5
res.rgate n9 n20 = 3.77
res.rslc1 n5 n51 = 1e-6, tc1=1.8e-3,tc2=1.7e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 5.5e-3, tc1=1e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-5.3e-3,tc2=-1.0e-5
res.rvtemp n18 n19 = 1, tc1=-2.5e-3,tc2=1e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/160))** 6))
}



SPICE Thermal Model

REV 23 March 2002

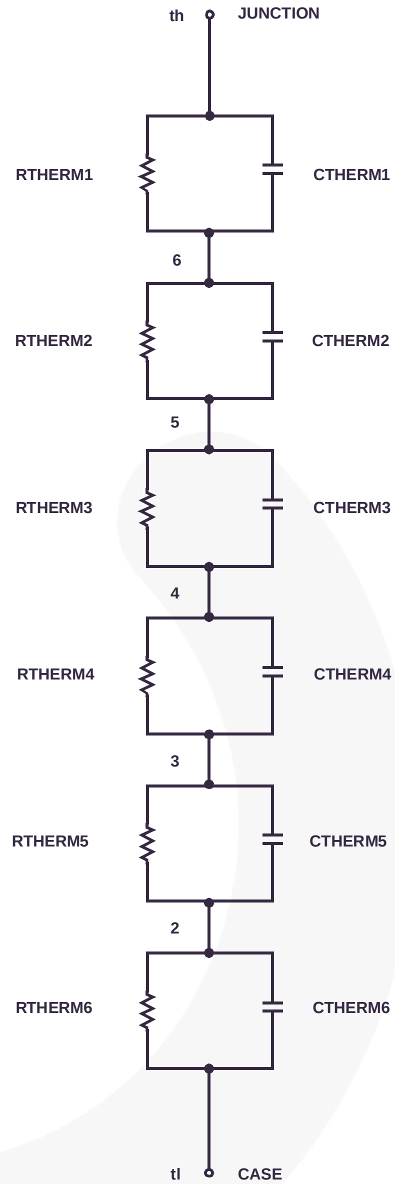
FDB13AN06A0T
CTHERM1 TH 6 9.7e-4
CTHERM2 6 5 6.2e-3
CTHERM3 5 4 4.6e-3
CTHERM4 4 3 4.9e-3
CTHERM5 3 2 8e-3
CTHERM6 2 TL 4.2e-2

RTHERM1 TH 6 5.24e-2
RTHERM2 6 5 10.08e-2
RTHERM3 5 4 4.28e-1
RTHERM4 4 3 1.8e-1
RTHERM5 3 2 1.9e-1
RTHERM6 2 TL 2.1e-1

SABER Thermal Model

SABER thermal model FDB14AN06A0T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =9.7e-4
ctherm.ctherm2 6 5 =6.2e-3
ctherm.ctherm3 5 4 =4.6e-3
ctherm.ctherm4 4 3 =4.9e-3
ctherm.ctherm5 3 2 =8e-3
ctherm.ctherm6 2 tl =4.2e-2

rtherm.rtherm1 th 6 =5.24e-2
rtherm.rtherm2 6 5 =10.08e-2
rtherm.rtherm3 5 4 =4.28e-1
rtherm.rtherm4 4 3 =1.8e-1
rtherm.rtherm5 3 2 =1.9e-1
rtherm.rtherm6 2 tl =2.1e-1
}



Mechanical Dimensions

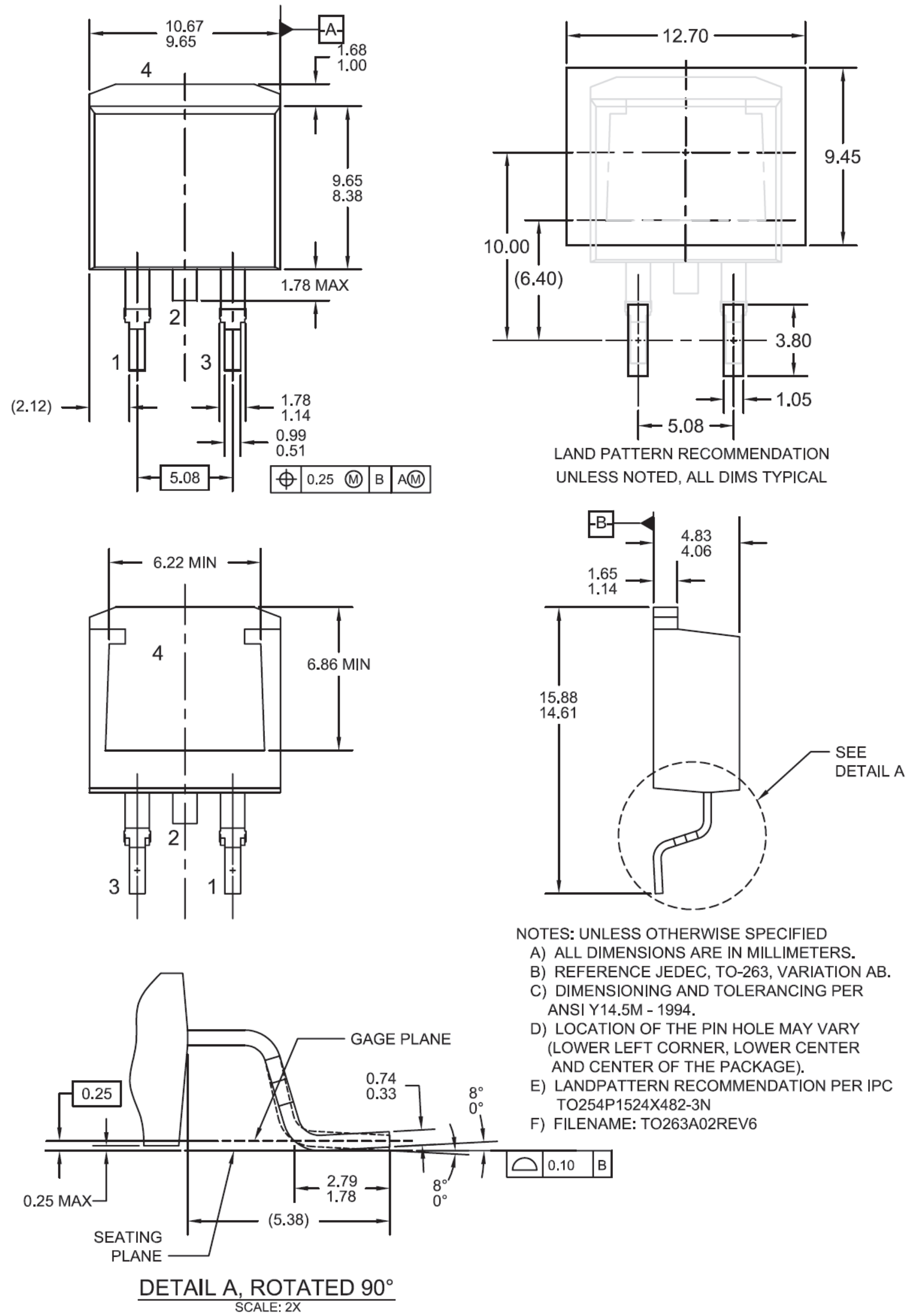


Figure 22. TO263 (D^2PAK), Molded, 2-Lead, Surface Mount

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