Low Power, Rail-to-Rail, Output Precision JFET Amplifier

AD8643-EP

FEATURES

- Low supply current: 250 µA maximum
- Very low input bias current: 1 pA maximum
- Low offset voltage: 750 µV maximum
- Single-supply operation: 5 V to 26 V
- Dual-supply operation: ±2.5 V to ±13 V
- Rail-to-rail output
- Unity-gain stable
- No phase reversal

PIN CONFIGURATION

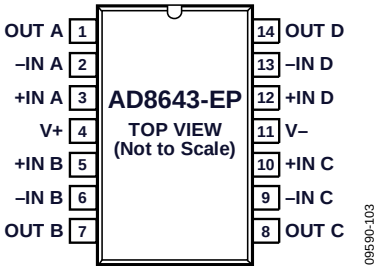

Figure 1. 14-Lead SOIC (R-14)

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Line-/battery-powered instruments
- Photodiode amplifiers
- Precision current sensing
- Precision filters
- Portable audio

GENERAL DESCRIPTION

The AD8643-EP is a low power, precision JFET input amplifier featuring extremely low input bias current and rail-to-rail output. The ability to swing nearly rail-to-rail at the input and rail-to-rail at the output enables designers to buffer CMOS digital-to-analog converters (DACs), ASICs, and other wide output swing devices in single-supply systems. The outputs remain stable with capacitive loads of more than 500 pF.

The AD8643-EP is suitable for applications using multichannel boards that require low power to manage heat. Other applications include photodiodes and battery management.

The AD8643-EP is fully specified over the military temperature range of −55°C to +125°C. This device is available in a 14-lead SOIC.

Additional applications information is available in the AD8643 data sheet.

Rev. 0

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REVISION HISTORY

1/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	1000	µV
		−55°C < T_A < +85°C			1.8	mV
		+85°C < T_A < +125°C, V_{CM} = 1.5 V			1.9	mV
Input Bias Current	I_B			0.25	1	pA
		−55°C < T_A < +125°C			180	pA
Input Offset Current	I_{OS}				0.5	pA
		−55°C < T_A < +125°C			60	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	74	93		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 to 4.5 V	80	140		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		4.95			V
		I_L = 1 mA, −55°C to +125°C	4.94			V
Output Voltage Low	V_{OL}				0.05	V
		I_L = 1 mA, −55°C to +125°C		0.01	0.05	V
Output Current	I_{OUT}			±6		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 26 V	90	107		dB
Supply Current/Amplifier	I_{SY}			195	250	µA
		−55°C < T_A < +125°C			270	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			2		V/µs
Gain Bandwidth Product	GBP			2.5		MHz
Phase Margin	$Ø_m$			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.0		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		28.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

V_S= ±13 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			70	1000	µV
		−55° < T_A < +125°C			1.8	mV
Input Bias Current	I_B			0.25	1	pA
		−55°C < T_A < +125°C			260	pA
Input Offset Current	I_{OS}				0.5	pA
		−55°C < T_A < +125°C			65	pA
Input Voltage Range			−13		+10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13 V to +10 V	90	107		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −11 V to +11 V	215	290		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C < T_A < +125°C		2.5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}		12.95			V
		I_L = 1 mA, −55°C to +125°C	12.94			V
Output Voltage Low	V_{OL}				−12.95	V
		I_L = 1 mA, −55°C to +125°C			−12.94	V
Output Current	I_{OUT}			±12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±13 V	90	107		dB
Supply Current/Amplifier	I_{SY}			200	290	µA
		−55°C < T_A < +125°C			330	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			3		V/µs
Gain Bandwidth Product	GBP			3.5		MHz
Phase Margin	$Ø_m$			60		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.2		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		27.5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	27.3 V
Input Voltage	V– to V+
Differential Input Voltage	±Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC (R)	120	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

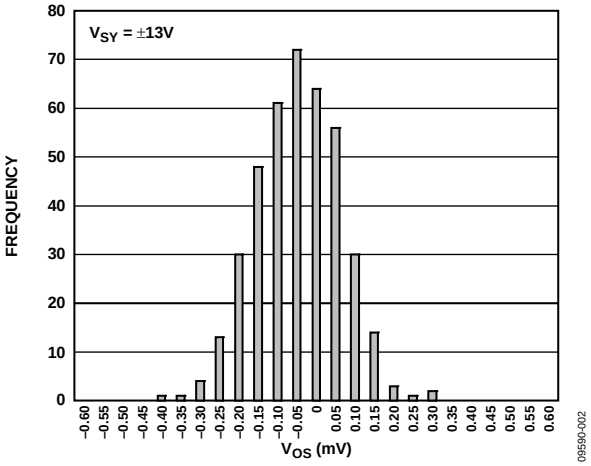


Figure 2. Input Offset Voltage

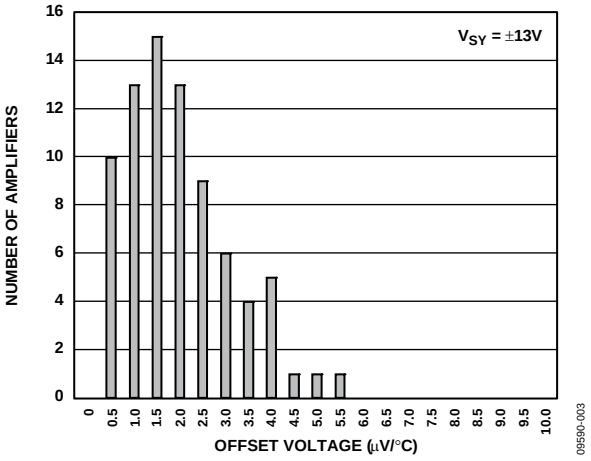


Figure 3. Offset Voltage Drift

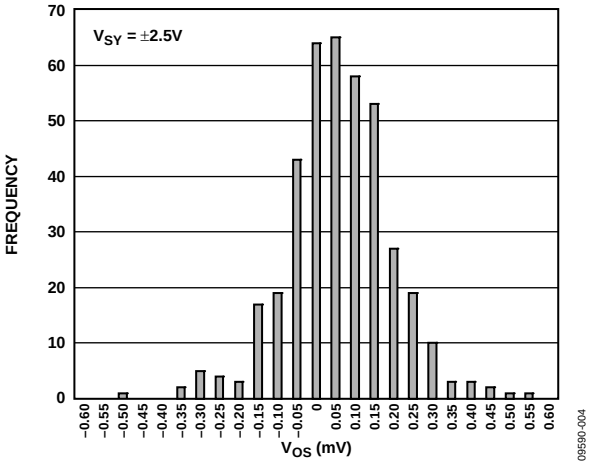


Figure 4. Input Offset Voltage

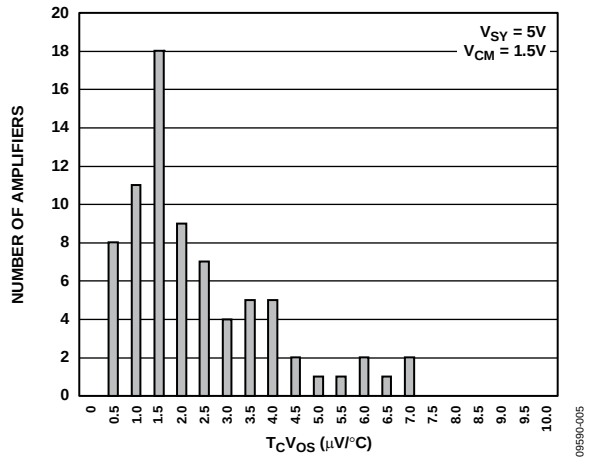


Figure 5. Offset Voltage Drift

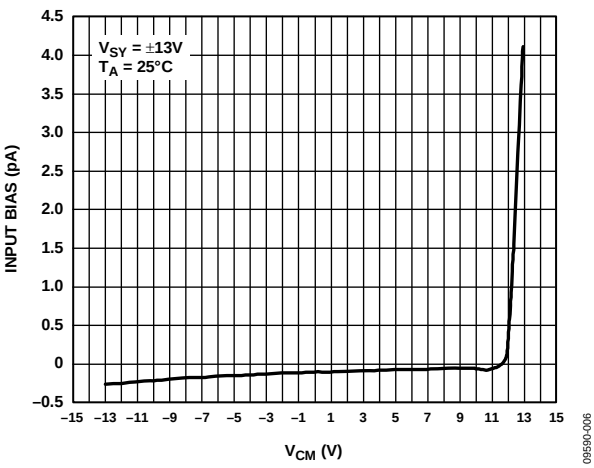


Figure 6. Input Bias Current vs. V_{CM}

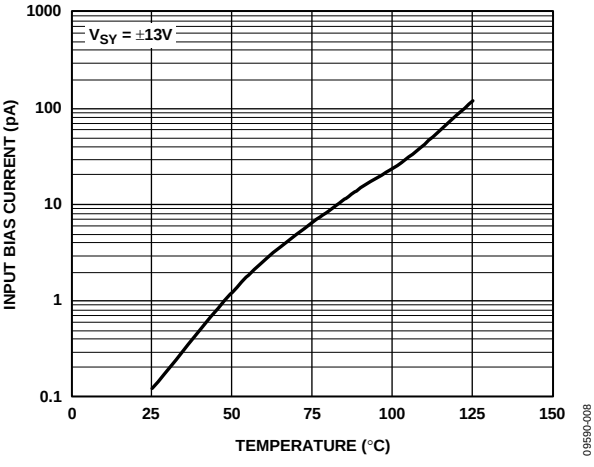


Figure 7. Input Bias Current vs. Temperature

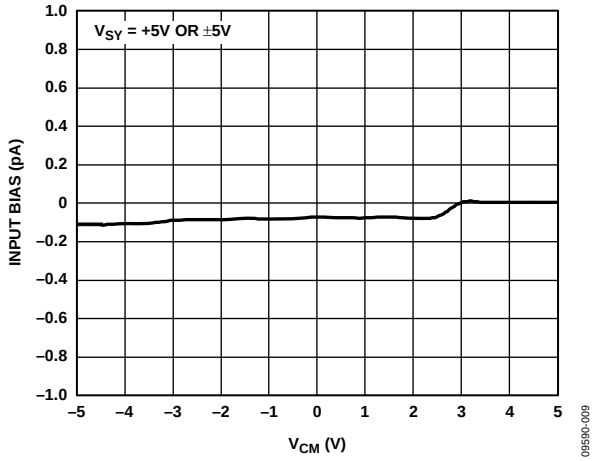


Figure 8. Input Bias Current vs. V_{CM}

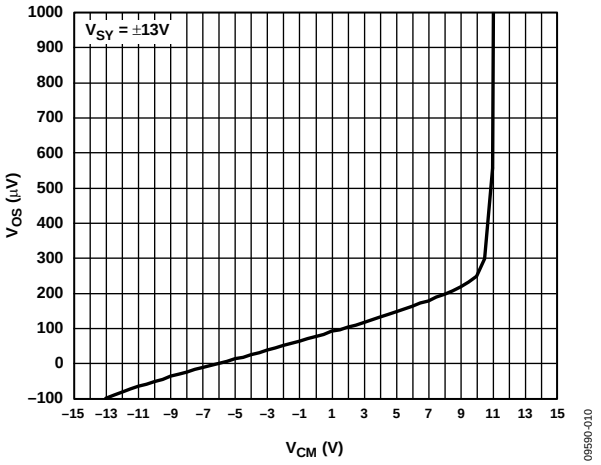


Figure 9. Input Offset Voltage (V_{OS}) vs. V_{CM}

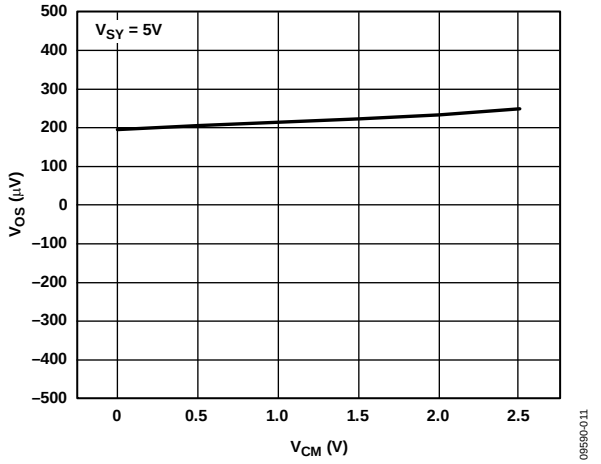


Figure 10. Input Offset Voltage vs. V_{CM}

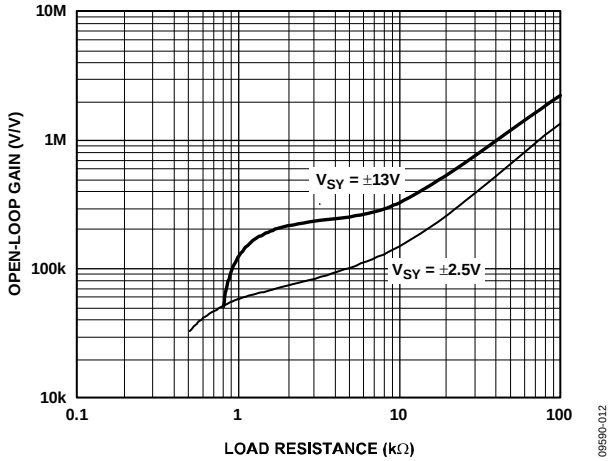


Figure 11. Open-Loop Gain vs. Load Resistance

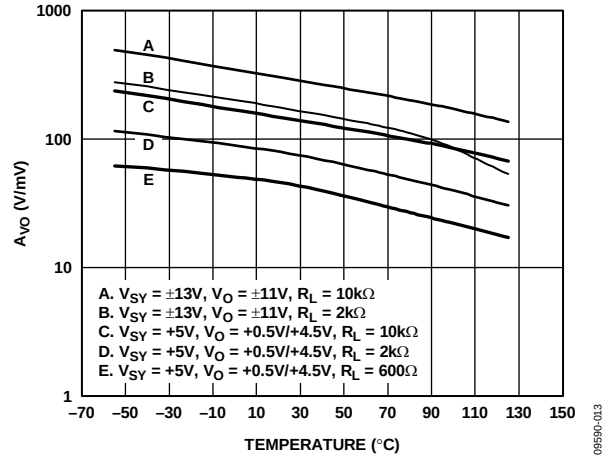


Figure 12. Open-Loop Gain vs. Temperature

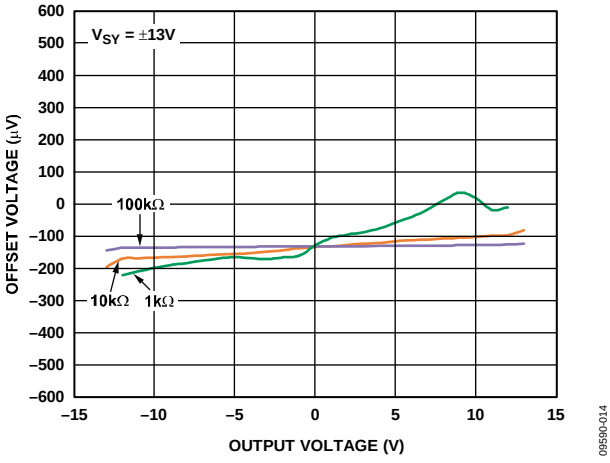


Figure 13. Input Error Voltage vs. Output Voltage for Resistive Loads

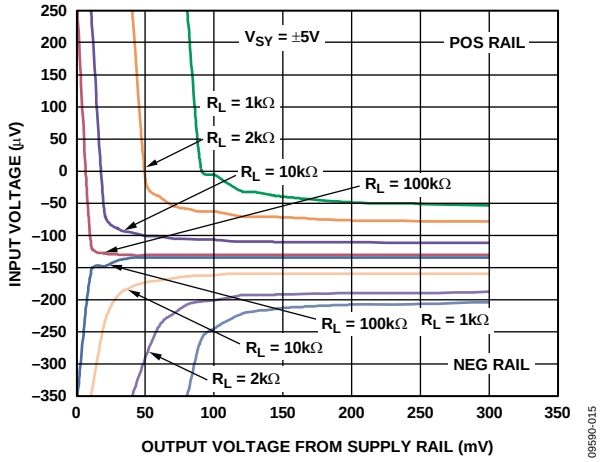


Figure 14. Input Error Voltage vs. Output Voltage Within 300 mV of Supply Rails

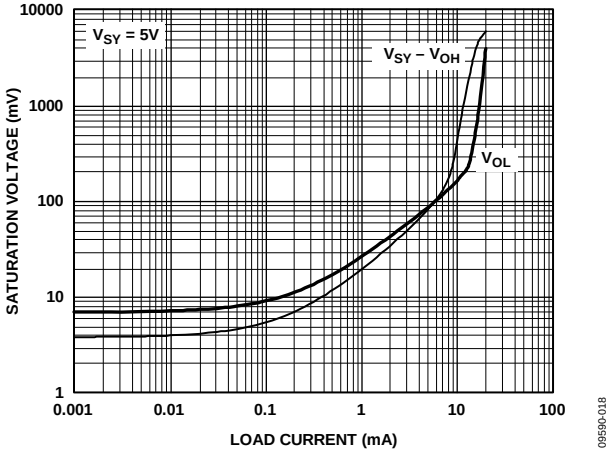
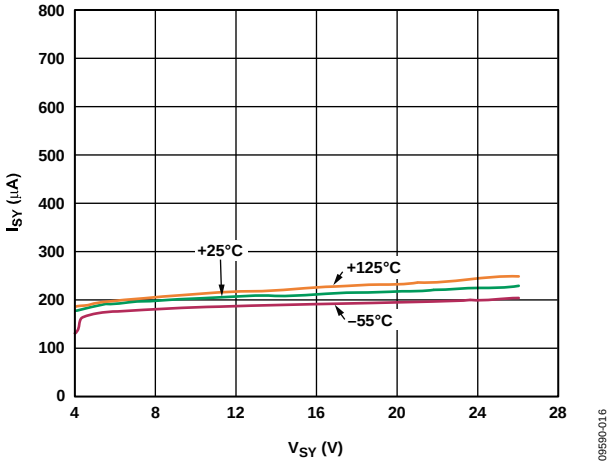


Figure 17. Output Saturation Voltage vs. Load Current



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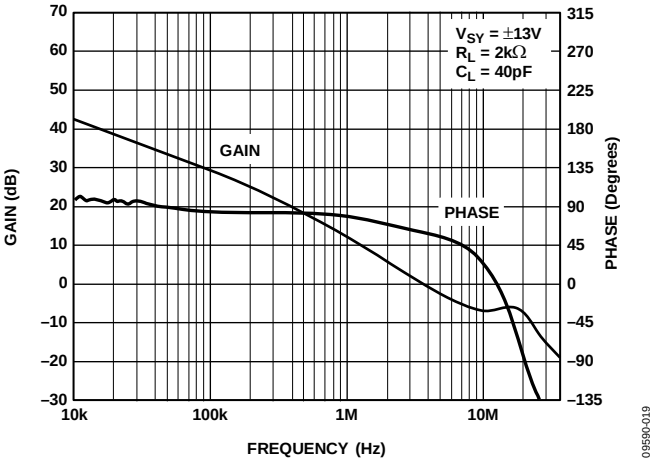


Figure 18. Open-Loop Gain and Phase Margin vs. Frequency

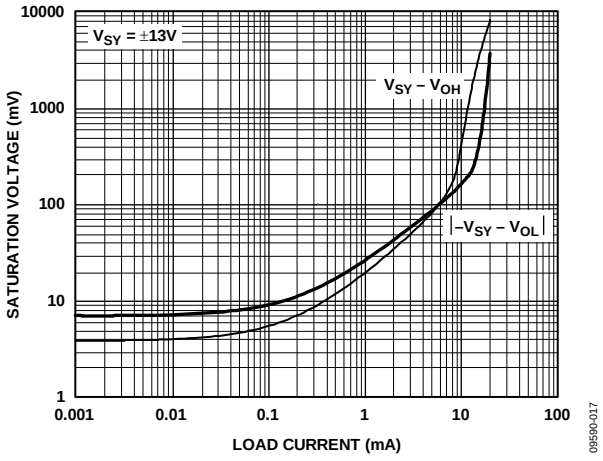


Figure 16. Output Saturation Voltage vs. Load Current

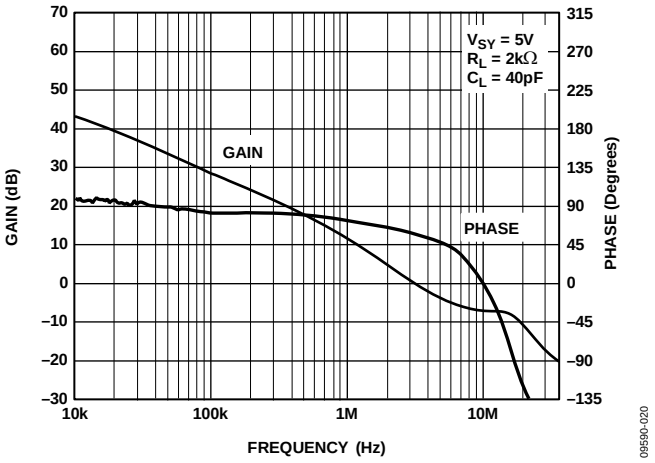


Figure 19. Open-Loop Gain and Phase Margin vs. Frequency

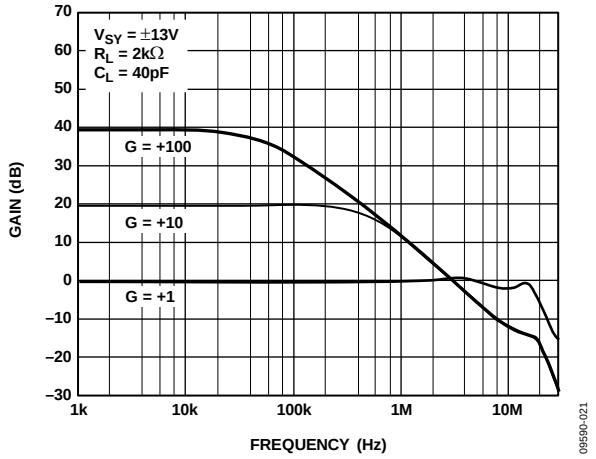


Figure 20. Closed-Loop Gain vs. Frequency

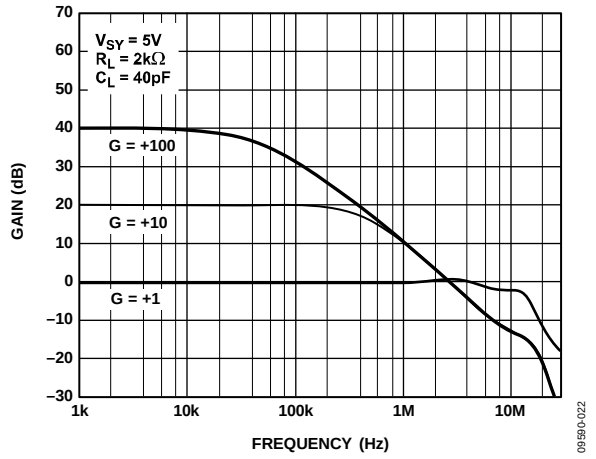


Figure 21. Closed-Loop Gain vs. Frequency

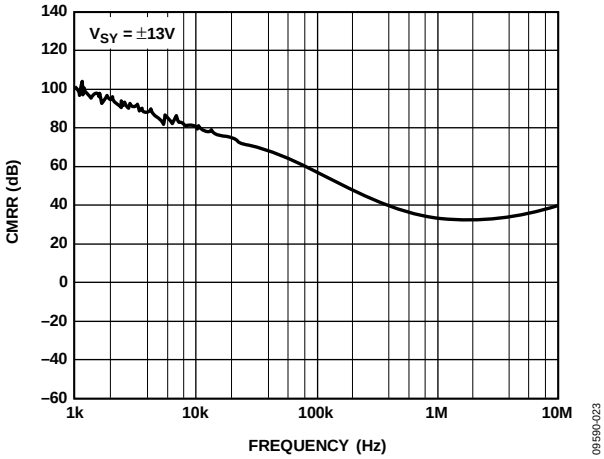


Figure 22. CMRR vs. Frequency

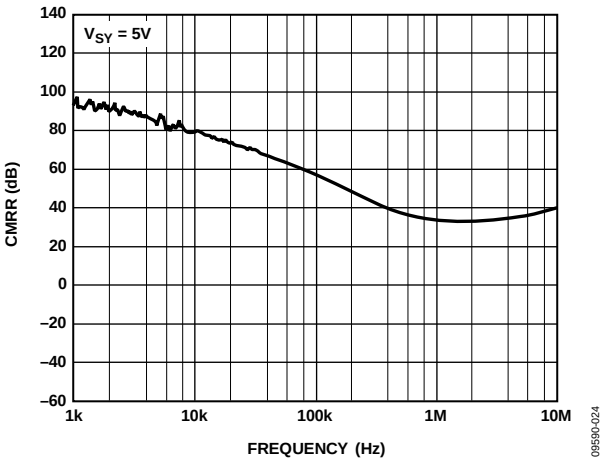


Figure 23. CMRR vs. Frequency

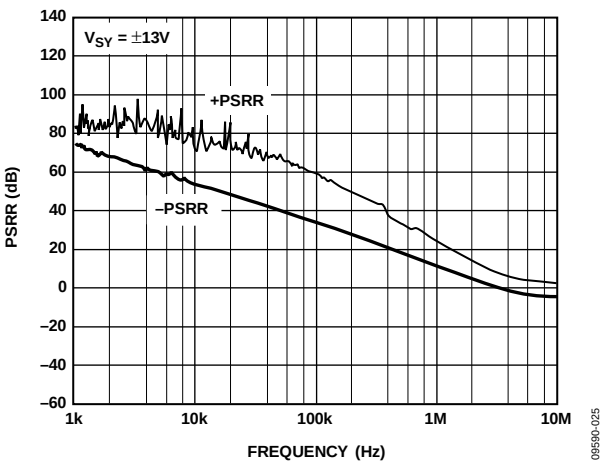


Figure 24. PSRR vs. Frequency

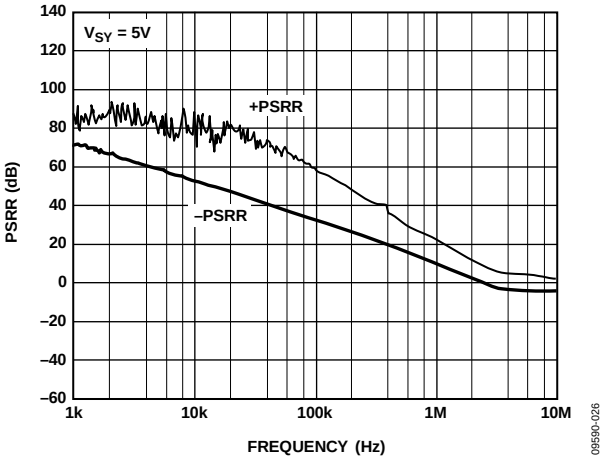


Figure 25. PSRR vs. Frequency

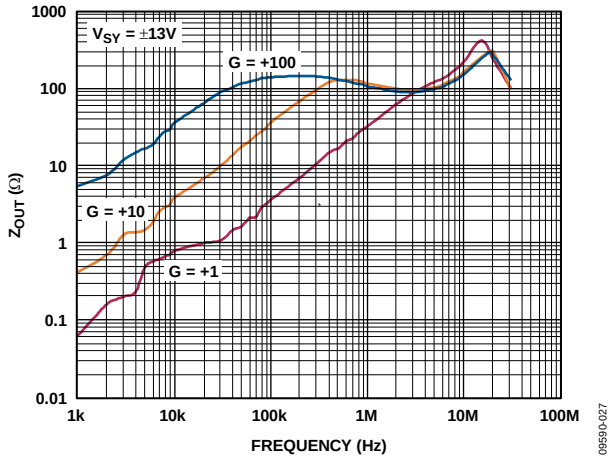


Figure 26. Output Impedance vs. Frequency

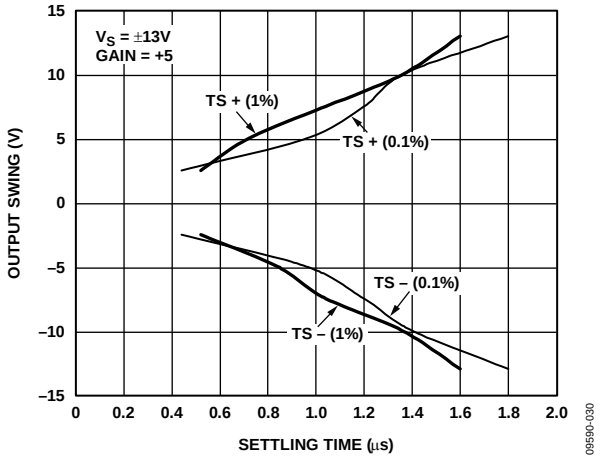


Figure 29. Output Swing and Error vs. Settling Time

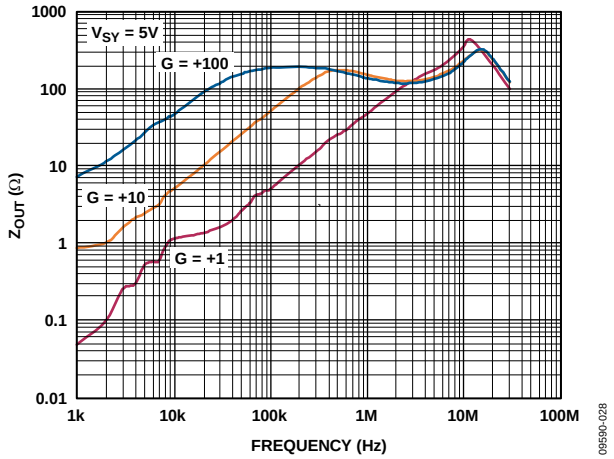


Figure 27. Output Impedance vs. Frequency

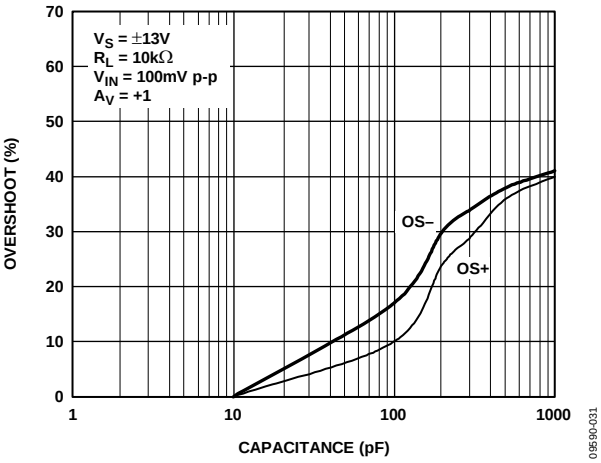


Figure 30. Small Signal Overshoot vs. Load Capacitance

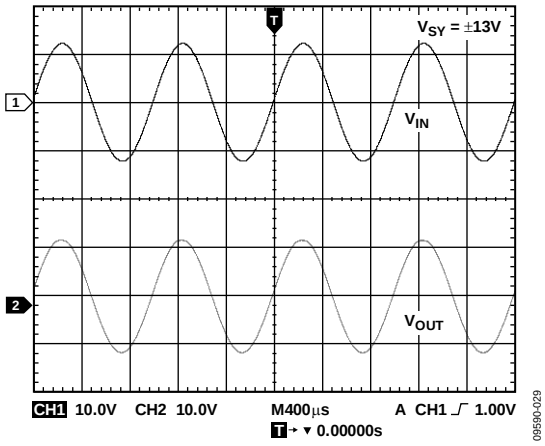


Figure 28. No Phase Reversal

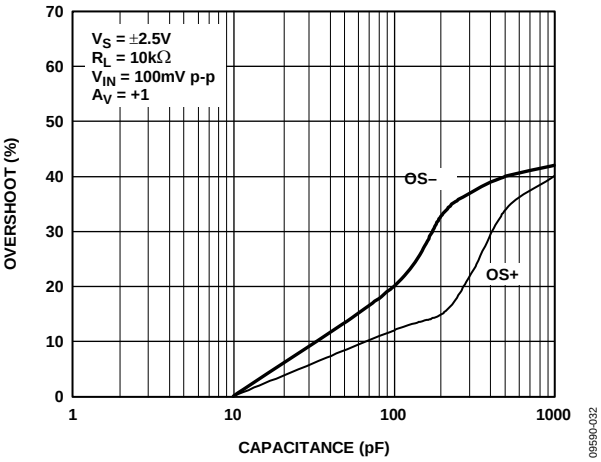


Figure 31. Small Signal Overshoot vs. Load Capacitance

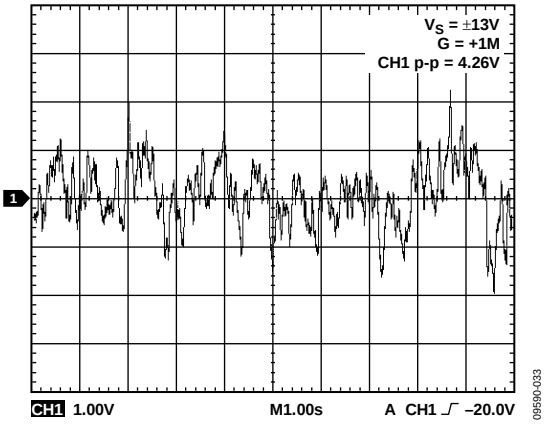


Figure 32. 0.1 Hz to 10 Hz Noise

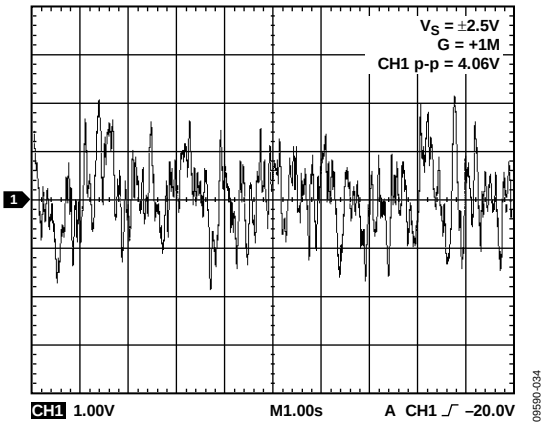


Figure 33. 0.1 Hz to 10 Hz Noise

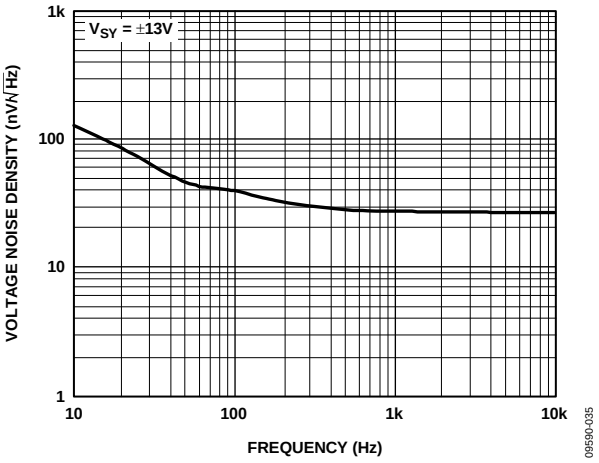


Figure 34. Voltage Noise Density

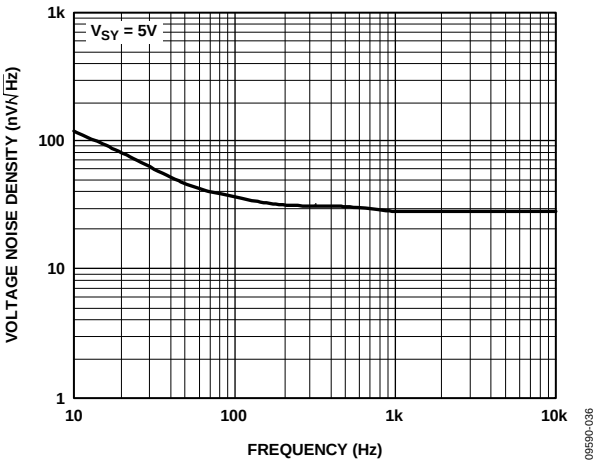


Figure 35. Voltage Noise Density

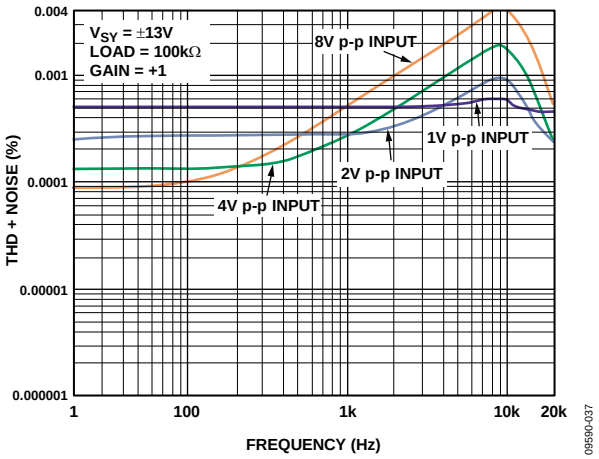


Figure 36. Total Harmonic Distortion + Noise vs. Frequency

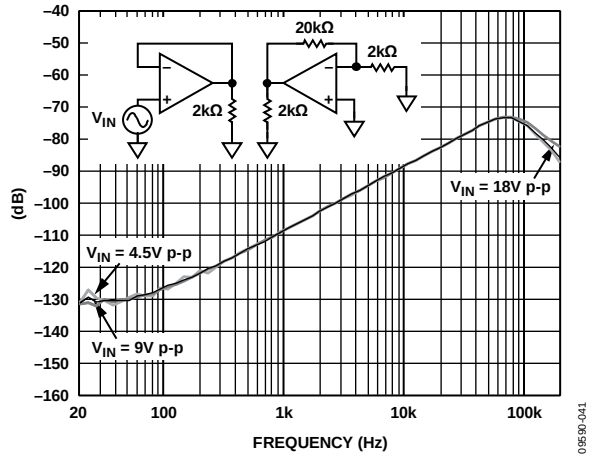
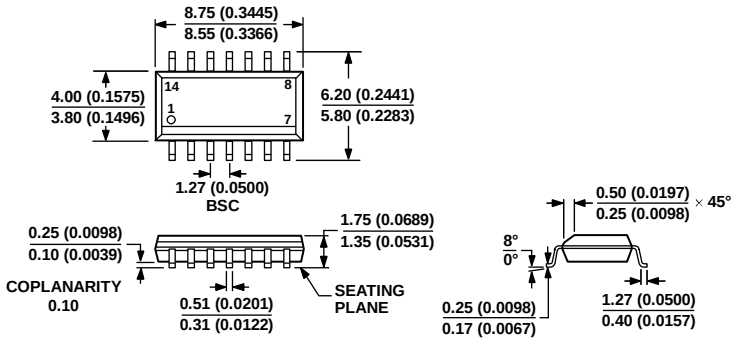


Figure 37. Channel Separation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 38. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8643TRZ-EP	−55°C to +125°C	14-lead SOIC_N	R-14
AD8643TRZ-EP-R7	−55°C to +125°C	14-lead SOIC_N	R-14

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

AD8641AKSZ-REEL AD8641ARZ-REEL AD8643TRZ-EP AD8643ARZ-REEL AD8641AKSZ-REEL7 AD8643TRZ-EP-R7 AD8641ARZ-REEL7 AD8642ARZ AD8641AKSZ-R2 AD8643ARZ-REEL7 AD8643ACPZ-REEL7 AD8643ARZ AD8643ACPZ-R2 AD8643ACPZ-REEL AD8642ARZ-REEL AD8642ARZ-REEL7 AD8642ARMZ-REEL AD8642ARMZ AD8641ARZ