14-Bit, 80 MSPS/105 MSPS A/D Converter

Data Sheet **AD6645**

FEATURES

SNR = 75 dB, f_{IN} 15 MHz, up to 105 MSPS
SNR = 72 dB, f_{IN} 200 MHz, up to 105 MSPS
SFDR = 89 dBc, f_{IN} 70 MHz, up to 105 MSPS
100 dBFS multitone SFDR
IF sampling to 200 MHz
Sampling jitter: 0.1 ps
1.5 W power dissipation
Differential analog inputs
Pin compatible to AD6644
Twos complement digital output format
3.3 V CMOS compatible
Data-ready for output latching

APPLICATIONS

Multichannel, multimode receivers
Base station infrastructures
AMPS, IS-136, CDMA, GSM, W-CDMA
Single channel digital receivers
Antenna array processing
Communications instrumentation
Radars, infrared imaging
Instrumentation

GENERAL DESCRIPTION

The AD6645 is a high speed, high performance, monolithic 14-bit analog-to-digital converter (ADC). All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution. The AD6645 provides CMOS-compatible digital outputs. It is the fourth generation in a wideband ADC family, preceded by the AD9042 (12-bit, 41 MSPS), the AD6640 (12-bit, 65 MSPS, IF sampling), and the AD6644 (14-bit, 40 MSPS/65 MSPS).

Designed for multichannel, multimode receivers, the AD6645 is part of the Analog Devices, Inc., SoftCell® transceiver chipset. The AD6645 maintains 100 dB multitone, spurious-free dynamic range (SFDR) through the second Nyquist band. This breakthrough performance eases the burden placed on multimode digital receivers (software radios) that are typically limited by the ADC. Noise performance is exceptional; typical signal-to-noise ratio (SNR) is 74.5 dB through the first Nyquist band.

The AD6645 is built on the Analog Devices extra fast complementary bipolar (XFCB) process and uses an innovative, multipass circuit architecture. Units are available in a 52-lead exposed pad (TQFP_EP) package specified from −40°C to +85°C at 80 MSPS and −10°C to +85°C at 105 MSPS.

PRODUCT HIGHLIGHTS

1. IF Sampling. The AD6645 maintains outstanding ac performance up to input frequencies of 200 MHz, suitable for multicarrier 3G wideband cellular IF sampling receivers.
2. Pin Compatibility. The ADC has the same footprint and pin layout as the AD6644 14-bit, 40 MSPS/65 MSPS ADC.
3. SFDR Performance and Oversampling. Multitone SFDR performance of 100 dBFS can reduce the requirements of high end RF components.

FUNCTIONAL BLOCK DIAGRAM

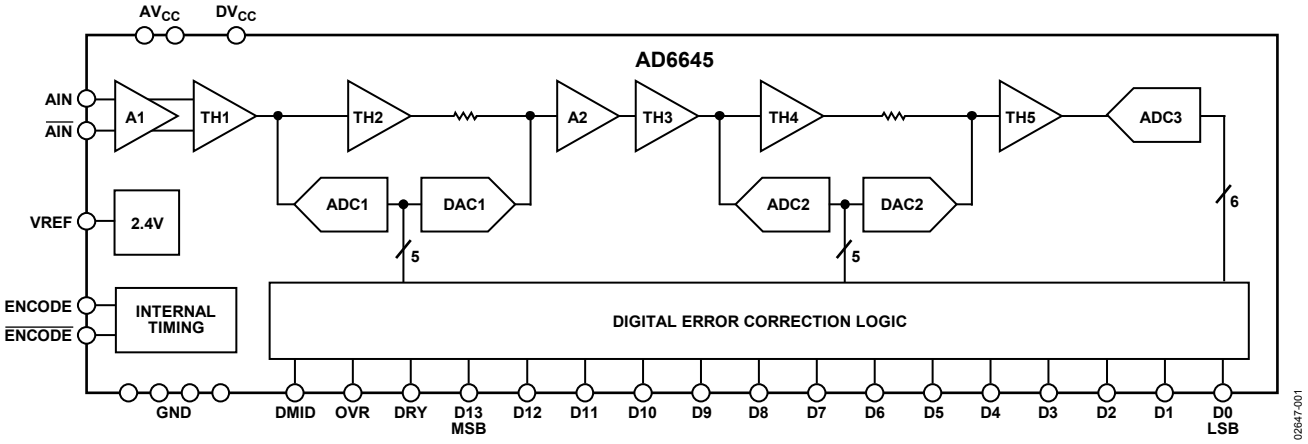

Figure 1.

Rev. E Document Feedback

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SPECIFICATIONS

DC SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.

Table 1.

			AD6645ASQ-80/AD6645ASV-80			AD6645ASQ-105/AD6645ASV-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				14			14		Bits
ACCURACY									
No Missing Codes	Full	II		Guaranteed			Guaranteed		
Offset Error	Full	II	−10	+1.2	+10	−10	+1.2	+10	mV
Gain Error	Full	II	−10	0	+10	−10	0	+10	% FS
Differential Nonlinearity (DNL)	Full	II	−1.0	±0.25	+1.5	−1.0	±0.5	+1.5	LSB
Integral Nonlinearity (INL)	Full	V		±0.5			±1.5		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		1.5			1.5		ppm/°C
Gain Error	Full	V		48			48		ppm/°C
POWER SUPPLY REJECTION RATIO (PSRR)	25°C	V		±1.0			±1.0		mV/V
REFERENCE OUT (VREF)[1]	Full	V		2.4			2.4		V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Differential Input Voltage Range	Full	V		2.2			2.2		V p-p
Differential Input Resistance	Full	V		1			1		kΩ
Differential Input Capacitance	25°C			1.5			1.5		pF
POWER SUPPLY									
Supply Voltages									
AV_{CC}	Full	II	4.75	5.0	5.25	4.75	5.0	5.25	V
DV_{CC}	Full	II	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
IAV_{CC} (AV_{CC} = 5.0 V)	Full	II		275	320		275	320	mA
IDV_{CC} (DV_{CC} = 3.3 V)	Full	II		32	45		32	45	mA
Rise Time[2]									
AV_{CC}	Full	IV			250		5.0	250	ms
POWER CONSUMPTION	Full	II		1.5	1.75		1.5	1.75	W

[1] VREF is provided for setting the common-mode offset of a differential amplifier, such as the AD8138, when a dc-coupled analog input is required. VREF should be buffered if used to drive additional circuit functions.
[2] Specified for dc supplies with linear rise time characteristics.

DIGITAL SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	AD6645ASQ-80/AD6645ASV-80 Min	Typ	Max	AD6645ASQ-105/AD6645ASV-105 Min	Typ	Max	Unit
ENCODE INPUTS (ENCODE, $\overline{\text{ENCODE}}$)									
Differential Input Voltage[1]	Full	IV	0.4			0.4			V p-p
Differential Input Resistance	25°C	V		10			10		kΩ
Differential Input Capacitance	25°C	V		2.5			2.5		pF
LOGIC OUTPUTS (D13 to D0, DRY, OVR)									
Logic Compatibility				CMOS			CMOS		
Logic 1 Voltage (DV_{CC} = 3.3 V)[2]	Full	II	2.85	DV_{CC} − 2		2.85	DV_{CC} − 2		V
Logic 0 Voltage (DV_{CC} = 3.3 V)[2]	Full	II		0.2	0.5		0.2	0.5	V
Output Coding				Twos complement			Twos complement		
DMID	Full	V		DV_{CC}/2			DV_{CC}/2		V

[1] All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.
[2] Digital output logic levels: DV_{CC} = 3.3 V, C_{LOAD} = 10 pF. Capacitive loads >10 pF degrades performance.

AC SPECIFICATIONS

All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially. AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{\text{ENCODE}}$, T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD6645ASQ-80/ AD6645ASV-80 Min	Typ	Max	AD6645ASQ-105/ AD6645ASV-105 Min	Typ	Max	Unit	Conditions
SNR										
Analog Input @ −1 dBFS	25°C	V		75.0			75.0		dB	At 15.5 MHz
	Full	II	72.5	74.5					dB	At 30.5 MHz
	25°C	I				72.5	74.5		dB	At 37.7 MHz
	Full	II	72.0	73.5		72.0	73.5		dB	At 70.0 MHz
	25°C	V		73.0			73.0		dB	At 150.0 MHz
	25°C	V		72.0			72.0		dB	At 200.0 MHz
SINAD										
Analog Input @ −1 dBFS	25°C	V		75.0			75.0		dB	At 15.5 MHz
	Full	II	72.5	74.5					dB	At 30.5 MHz
	25°C	I				72.5	74.5		dB	At 37.7 MHz
	Full	V		73.0			73.0		dB	At 70.0 MHz
	25°C	V		68.5			67.5		dB	At 150.0 MHz
	25°C	V		62.5			62.5		dB	At 200.0 MHz
WORST HARMONIC (SECOND OR THIRD)										
Analog Input @ −1 dBFS	25°C	V		93.0			93.1		dBc	At 15.5 MHz
	Full	II	85.0	93.0					dBc	At 30.5 MHz
	25°C	I				85.0	93.0		dBc	At 37.7 MHz
	Full	V		89.0			87.0		dBc	At 70.0 MHz
	25°C	V		70.0			70.0		dBc	At 150.0 MHz
	25°C	V		63.5			63.5		dBc	At 200.0 MHz

Parameter	Temp	Test Level	AD6645ASQ-80/ AD6645ASV-80 Min	Typ	Max	AD6645ASQ-105/ AD6645ASV-105 Min	Typ	Max	Unit	Conditions
WORST HARMONIC (FOURTH OR HIGHER)										
Analog Input @ −1 dBFS	25°C	V		96.0			96.0		dBc	At 15.5 MHz
	Full	II	85.0	95.0					dBc	At 30.5 MHz
	25°C	I				86.0	95.0		dBc	At 37.7 MHz
	Full	V		90.0			90.0		dBc	At 70.0 MHz
	25°C	V		90.0			90.0		dBc	At 150.0 MHz
	25°C	V		88.0			88.0		dBc	At 200.0 MHz
TWO-TONE SFDR	25°C	V		100			98.0		dBFS	At 30.5 MHz[1, 2]
	25°C	V		100			98.0		dBFS	At 55.0 MHz[1, 3]
	25°C	V					98.0		dBFS	At 70.0 MHz[1, 4]
TWO-TONE IMD REJECTION[2, 3]										
F1, F2 @ −7 dBFS	25°C	V		90			90		dBc	
ANALOG INPUT BANDWIDTH	25°C	V		270			270		MHz	

[1] Analog input signal power swept from −10 dBFS to −100 dBFS.
[2] F1 = 30.5 MHz, F2 = 31.5 MHz.
[3] F1 = 55.25 MHz, F2 = 56.25 MHz.
[4] F1 = 69.1 MHz, F2 = 71.1 MHz.

SWITCHING SPECIFICATIONS

AV_{CC} = 5 V, DV_{CC} = 3.3 V; ENCODE, $\overline{\text{ENCODE}}$, T_{MIN} and T_{MAX} at rated speed grade, unless otherwise noted.

Table 4.

Parameter	Symbol	Temp	Test Level	AD6645ASQ-80/ AD6645ASV-80 Min	Typ	Max	AD6645ASQ-105/ AD6645ASV-105 Min	Typ	Max	Unit
ENCODE INPUT PARAMETERS[1]										
Maximum Conversion Rate		Full	II	80			105			MSPS
Minimum Conversion Rate		Full	IV			30			30	MSPS
ENCODE Pulse Width High, t_{ENCH}[2]		Full	IV	5.625			4.286			ns
		Full	V		6.25			4.75		ns
ENCODE Pulse Width Low, t_{ENCL}[2]		Full	IV	5.625			4.286			ns
		Full	V		6.25			4.75		ns
ENCODE Period[1]	t_{ENC}	Full	V		12.5			9.5		ns
ENCODE/DATA-READY										
ENCODE Rising to Data-Ready Falling	t_{DR}	Full	V	1.0	2.0	3.1	1.0	2.0	3.1	ns
ENCODE Rising to Data-Ready Rising	t_{E_DR}	Full	V		$t_{ENCH} + t_{DR}$			$t_{ENCH} + t_{DR}$		ns
50% Duty Cycle		Full	V	7.3	8.3	9.4	5.7	6.75	7.9	ns
ENCODE/DATA (D13:0), OVR										
ENCODE to DATA Falling Low	t_{E_FL}	Full	V	2.4	4.7	7.0	2.4	4.7	7.0	ns
ENCODE to DATA Rising Low[3]	t_{E_RL}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay[3] (Hold Time)	t_{H_E}	Full	V	1.4	3.0	4.7	1.4	3.0	4.7	ns
ENCODE to DATA Delay (Setup Time)	t_{S_E}	Full	V	$t_{ENC} - t_{E\_FL(max)}$			$t_{ENC} - t_{E\_FL(max)}$			ns
					$t_{ENC} - t_{E\_FL(typ)}$			$t_{ENC} - t_{E\_FL(typ)}$		ns
						$t_{ENC} - t_{E\_FL(min)}$			$t_{ENC} - t_{E\_FL(min)}$	ns
50% Duty Cycle		Full	V	5.3	7.6	10.0	2.3	4.8	7.0	ns

Parameter	Symbol	Temp	Test Level	AD6645ASQ-80/ AD6645ASV-80 Min	Typ	Max	AD6645ASQ-105/ AD6645ASV-105 Min	Typ	Max	Unit
DATA-READY (DRY[4])/DATA(D13:0),, OVR										
Data-Ready to DATA Delay (Hold Time)	t_{H_DR}	Full	V		Note 5[5]			Note 5[5]		
50% Duty Cycle		Full	V	6.6	7.2	7.9	5.1	5.7	6.4	ns
Data-Ready to DATA Delay (Setup Time)	t_{S_DR}	Full	V		Note 5[5]			Note 5[5]		
50% Duty Cycle		Full	V	2.1	3.6	5.1	0.6	2.1	3.5	ns
APERTURE DELAY	t_A	25°C	V		−500			−500		ps
APERTURE UNCERTAINTY (JITTER)	t_J	25°C	V		0.1		0.1			ps rms

[1] Several timing parameters are a function of t_{ENC} and t_{ENCH}.
[2] Several timing parameters are a function of t_{ENCL} and t_{ENCH}.
[3] ENCODE TO DATA Delay (Hold Time) is the absolute minimum propagation delay through the ADC, $t_{E\_RL} = t_{H\_E}$.
[4] DRY is an inverted and delayed version of the encode clock. Any change in the duty cycle of the clock will correspondingly change the duty cycle of DRY.
[5] Data-ready to DATA Delay (t_{H_DR} and t_{S_DR}) is calculated relative to rated speed grade and is dependent on t_{ENC} and duty cycle.

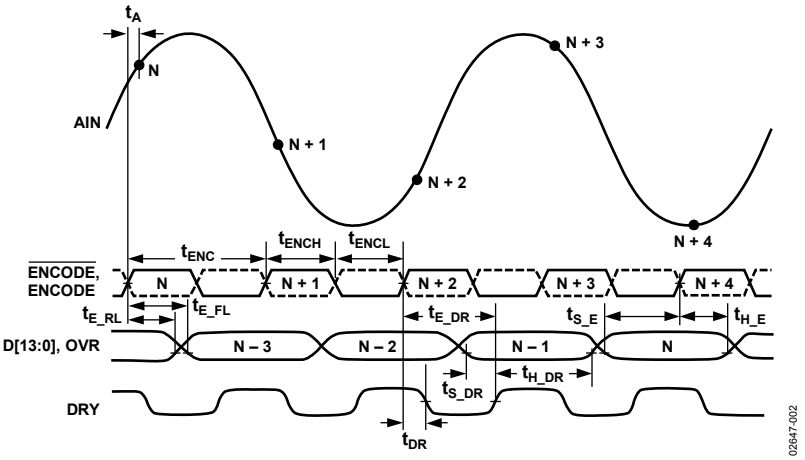

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
AV_{CC} Voltage	0 V to 7 V
DV_{CC} Voltage	0 V to 7 V
Analog Input Voltage	0 V to AV_{CC}
Analog Input Current	25 mA
Digital Input Voltage	0 V to AV_{CC}
Digital Output Current	4 mA
Environmental	
Operating Temperature Range (Ambient)	
AD6645-80	−40°C to +85°C
AD6645-105	−10°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The heat sink of the AD6645ASVZ, 52-lead TQFP_EP (SV-52-1) package must be soldered to the PCB GND plane to meet thermal specifications.

Table 6. Thermal Characteristics

Package Type	Rating
52-Lead TQFP_EP	
θ_{JA} (0 m/sec airflow)[1, 2, 3]	23°C/W, soldered heat sink
θ_{JMA} (1.0 m/sec airflow)[2, 3, 4, 5]	17°C/W, soldered heat sink
θ_{JC}[6, 7]	2°C/W, soldered heat sink

[1] Per JEDEC JESD51-2 (heat sink soldered to PCB).
[2] 2S2P JEDEC test board.
[3] Values of θ_{JA} are provided for package comparison and PCB design considerations.
[4] Per JEDEC JESD51-6 (heat sink soldered to PCB).
[5] Airflow increases heat dissipation, effectively reducing θ_{JA}. Furthermore, the more metal that is directly in contact with the package leads from metal traces, throughholes, ground, and power planes, the more θ_{JA} is reduced.
[6] Per MIL-STD-883, Method 1012.1.
[7] Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where:

T_A is the ambient temperature (°C).

PD is the power dissipation (W).

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and guaranteed by design and characterization at temperature extremes.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

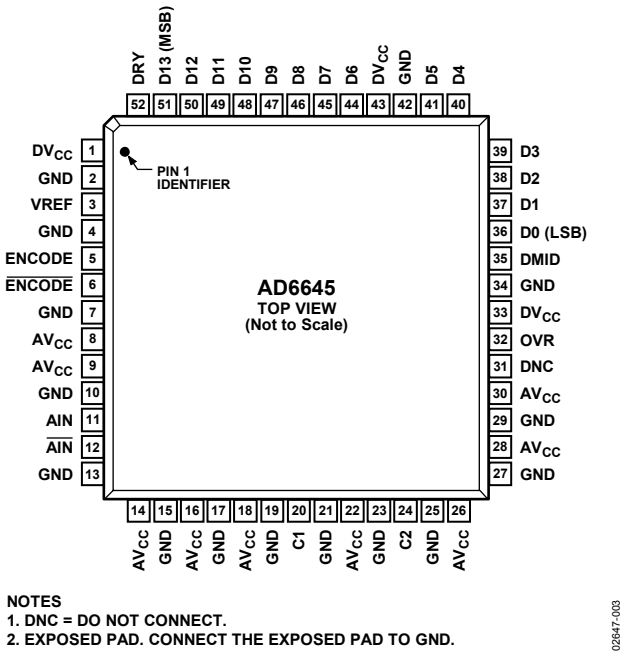

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 33, 43	DV_{CC}	3.3 V Power Supply (Digital) Output Stage Only.
2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	GND	Ground.
3	VREF	2.4 V Reference. Bypass to ground with a 0.1 µF microwave chip capacitor.
5	ENCODE	Encode Input. Conversion initiated on rising edge.
6	$\overline{\text{ENCODE}}$	Complement of $\overline{\text{ENCODE}}$, Differential Input.
8, 9, 14, 16, 18, 22, 26, 28, 30	AV_{CC}	5 V Analog Power Supply.
11	AIN	Analog Input.
12	$\overline{\text{AIN}}$	Complement of AIN, Differential Analog Input.
20	C1	Internal Voltage Reference. Bypass to ground with a 0.1 µF chip capacitor.
24	C2	Internal Voltage Reference. Bypass to ground with a 0.1 µF chip capacitor.
31	DNC	Do not connect this pin.
32	OVR	Overrange Bit. A logic level high indicates analog input exceeds ±FS.
35	DMID	Output Data Voltage Midpoint. Approximately equal to (DV_{CC})/2.
36	D0 (LSB)	Digital Output Bit (Least Significant Bit); Twos Complement.
37 to 41, 44 to 50	D1 to D5, D6 to D12	Digital Output Bits in Twos Complement.
51	D13 (MSB)	Digital Output Bit (Most Significant Bit); Twos Complement.
52	DRY	Data-Ready Output.
53 (EPAD)	Exposed Paddle (EPAD)	Exposed Pad. Connect the exposed pad to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

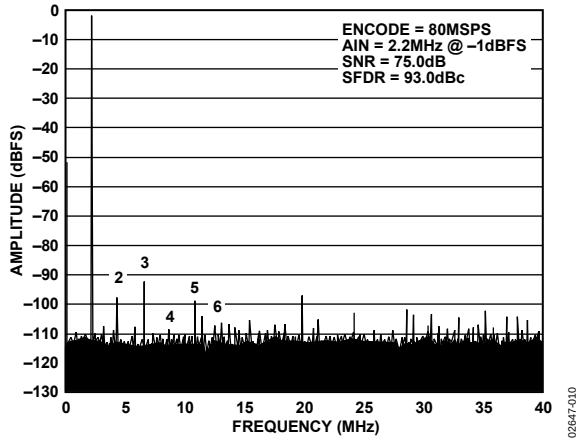

Figure 4. Single Tone @ 2.2 MHz

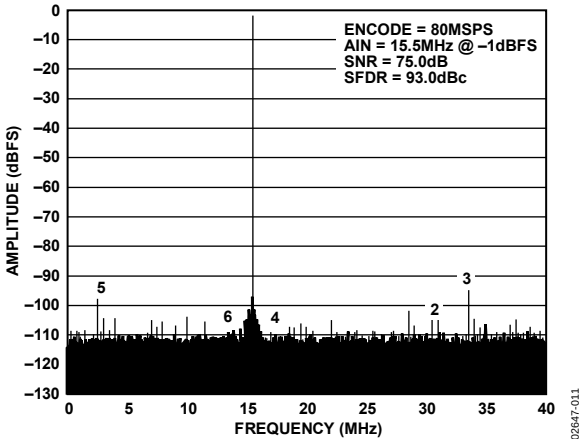

Figure 5. Single Tone @ 15.5 MHz

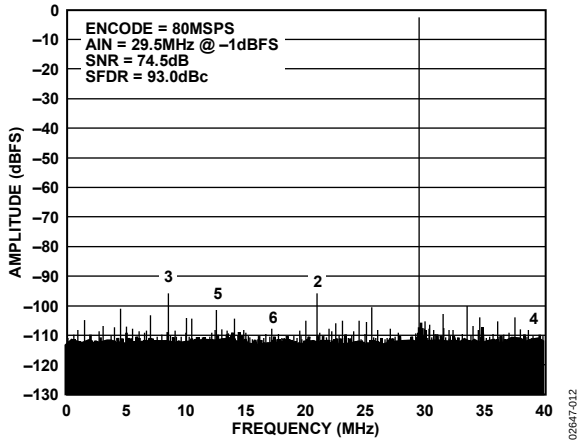

Figure 6. Single Tone @ 29.5 MHz

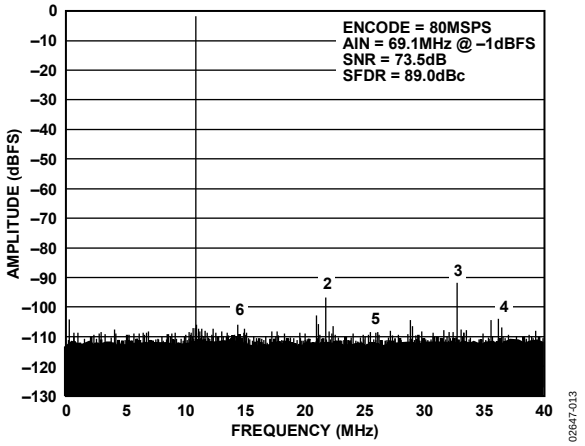

Figure 7. Single Tone @ 69.1 MHz

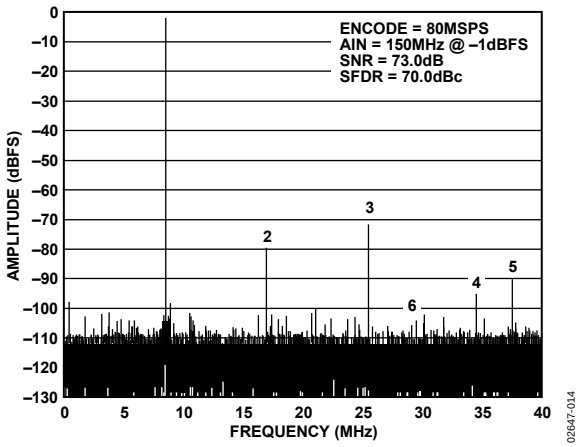

Figure 8. Single Tone @ 150 MHz

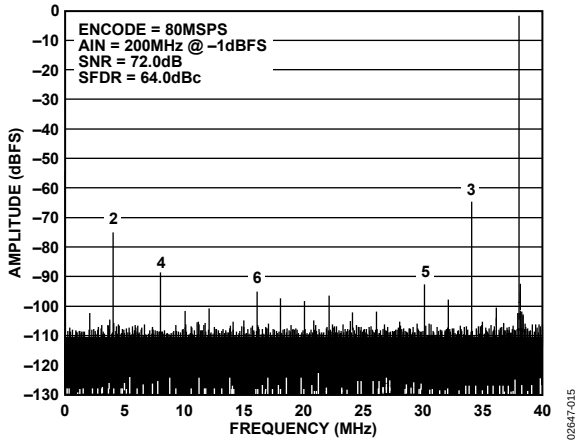

Figure 9. Single Tone @ 200 MHz

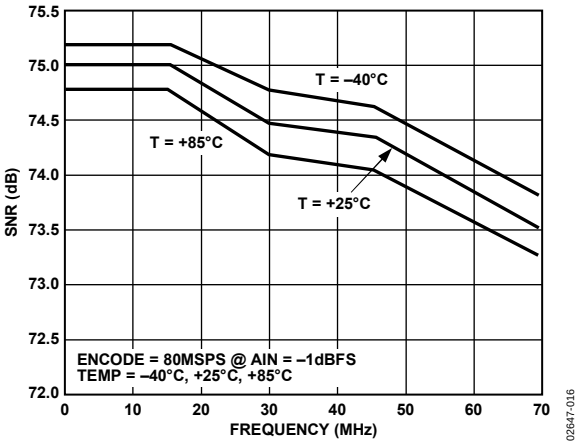

Figure 10. Signal-to-Noise Ratio (SNR) vs. Frequency

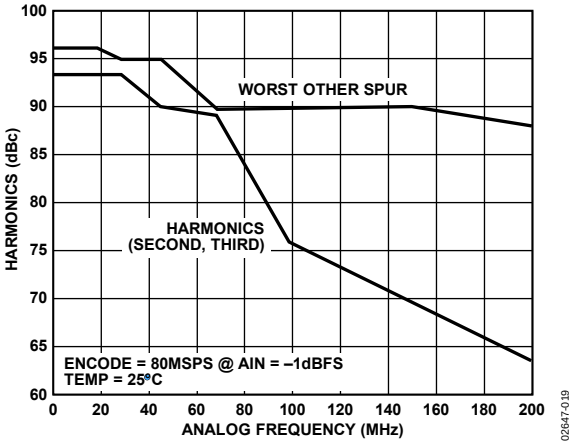

Figure 13. Harmonics vs. Analog Frequency (IF)

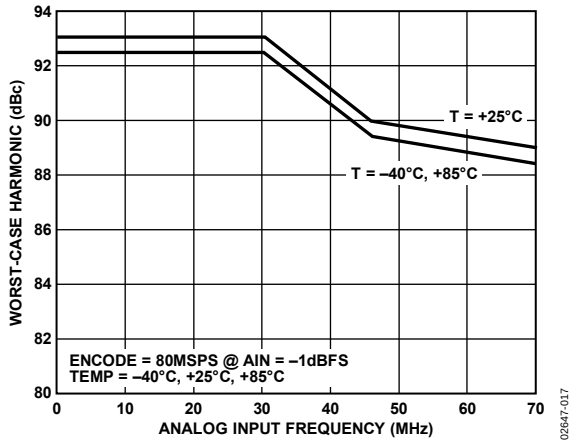

Figure 11. Worst-Case Harmonics vs. Analog Input Frequency

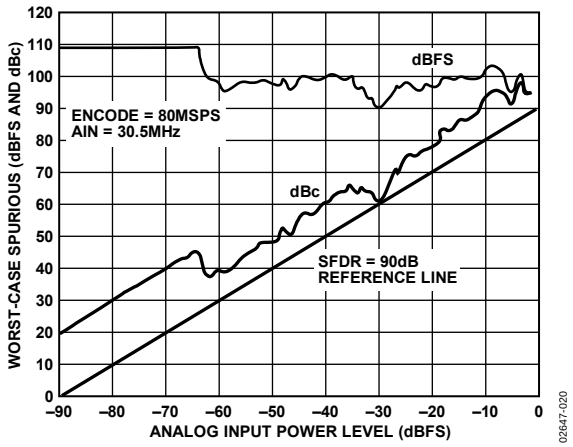

Figure 14. Single-Tone SFDR @ 30.5 MHz

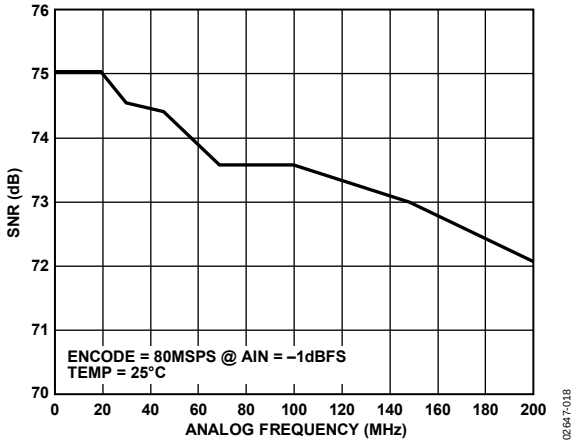

Figure 12. Signal-to-Noise Ratio (SNR) vs. Analog Frequency (IF)

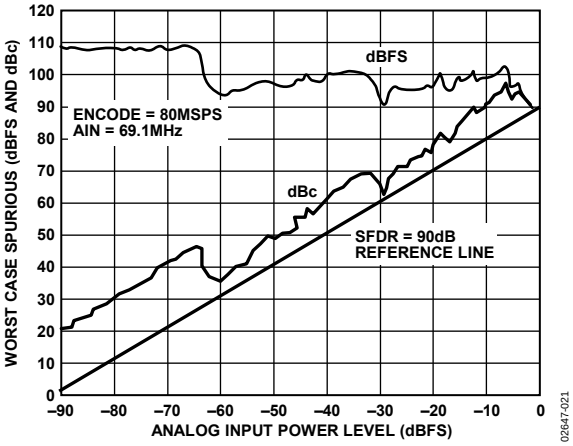

Figure 15. Single-Tone SFDR @ 69.1 MHz

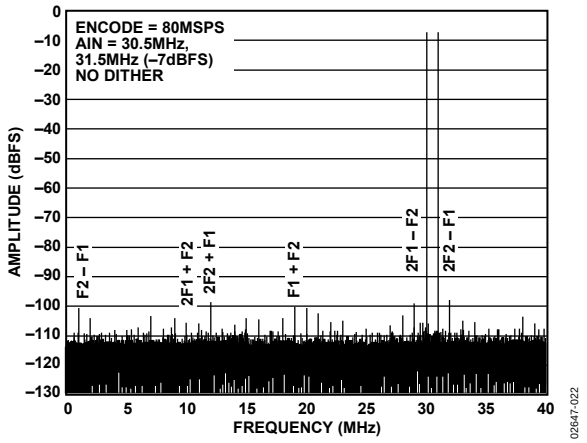

Figure 16. Two-Tone SFDR @ 30.5 MHz and 31.5 MHz

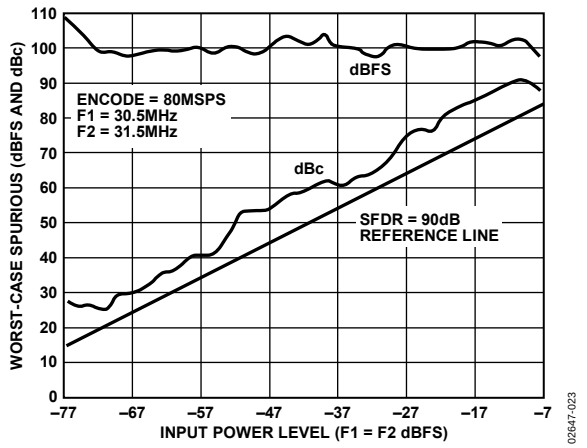

Figure 17. Two-Tone SFDR @ 30.5 MHz and 31.5 MHz

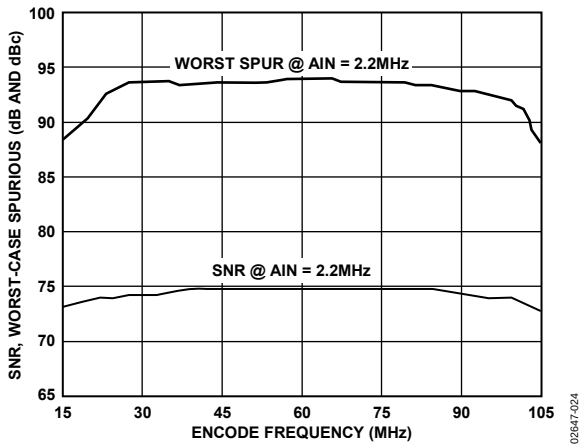

Figure 18. SNR, Worst-Case Spurious vs. Encode @ 2.2 MHz

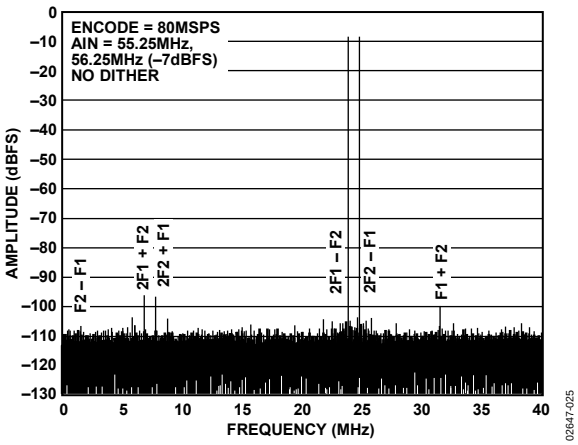

Figure 19. Two-Tone SFDR @ 55.25 MHz and 56.25 MHz

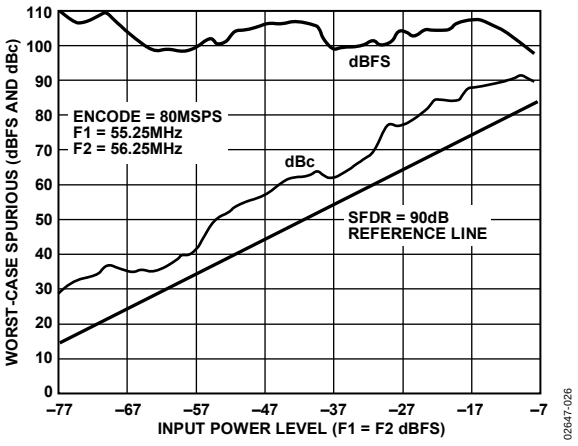

Figure 20. Two-Tone SFDR @ 55.25 MHz and 56.25 MHz

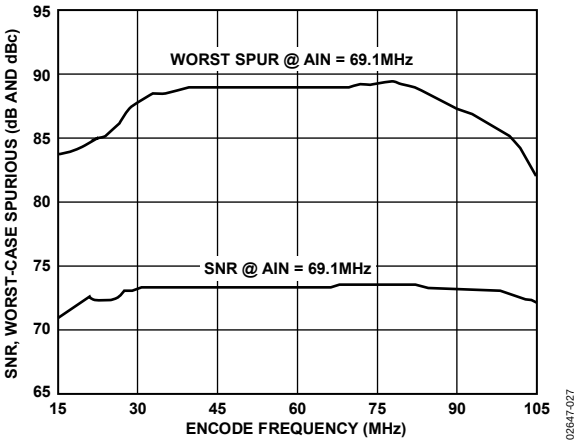

Figure 21. SNR, Worst-Case Spurious vs. Encode @ 69.1 MHz

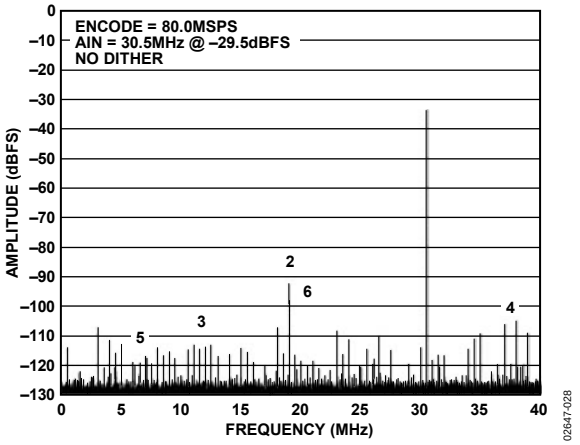

Figure 22. 1 M Sample FFT Without Dither

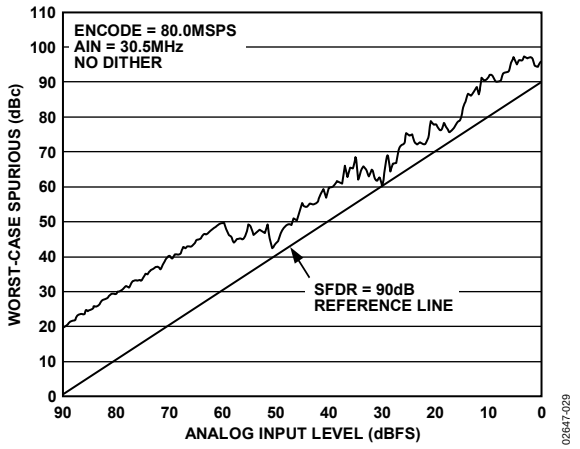

Figure 23. SFDR Without Dither

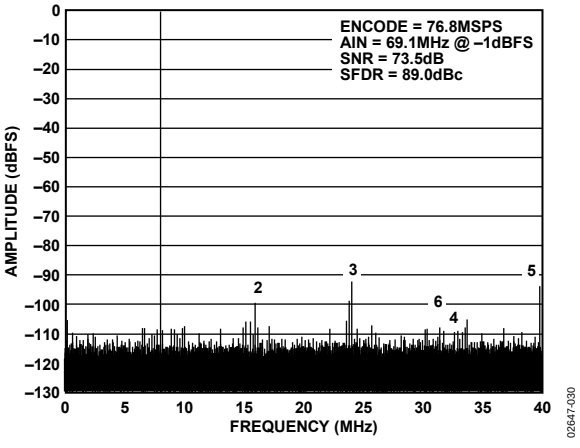

Figure 24. Single Tone @ 69.1 MHz, Encode = 76.8 MSPS

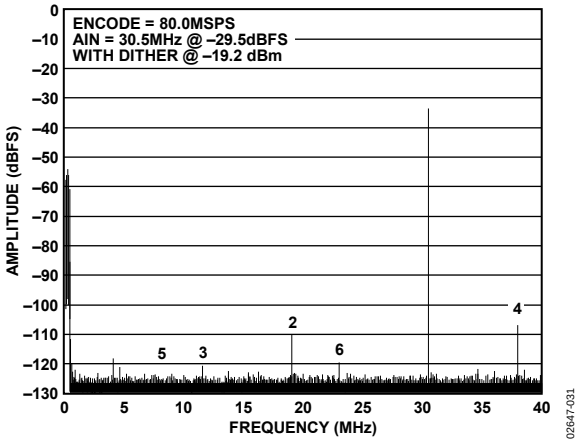

Figure 25. 1 M Sample FFT with Dither

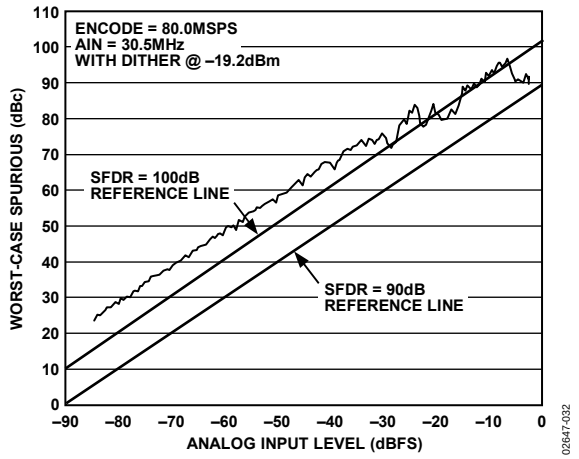

Figure 26. SFDR with Dither

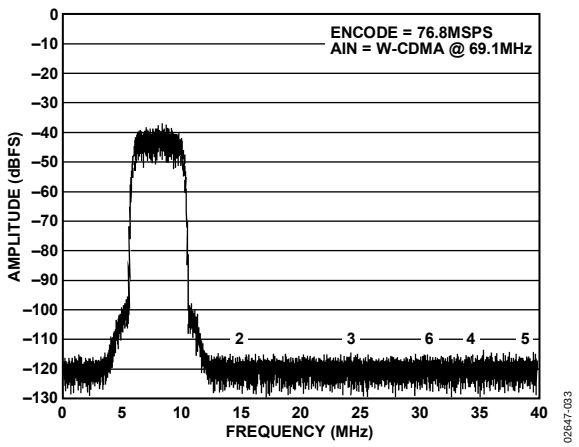

Figure 27. W-CDMA Tone @ 69.1 MHz, Encode = 76.8 MSPS

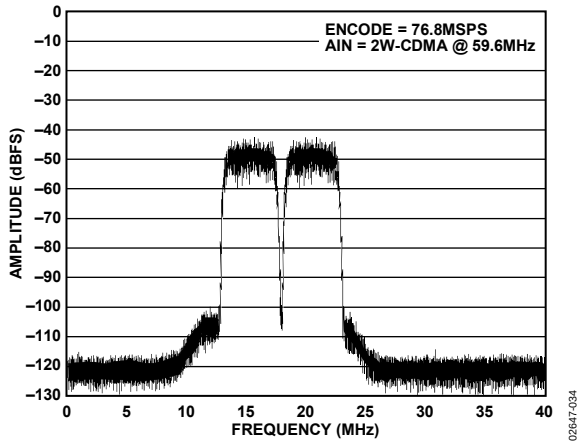

Figure 28. Two W-CDMA Carriers @ 59.6 MHz, Encode = 76.8 MSPS

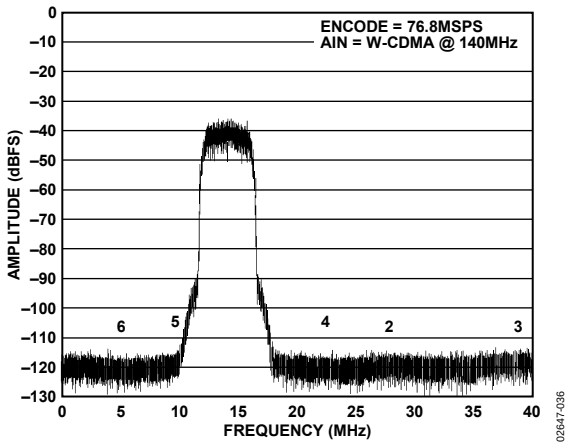

Figure 30. W-CDMA Tone @ 140 MHz, Encode = 76.8 MSPS

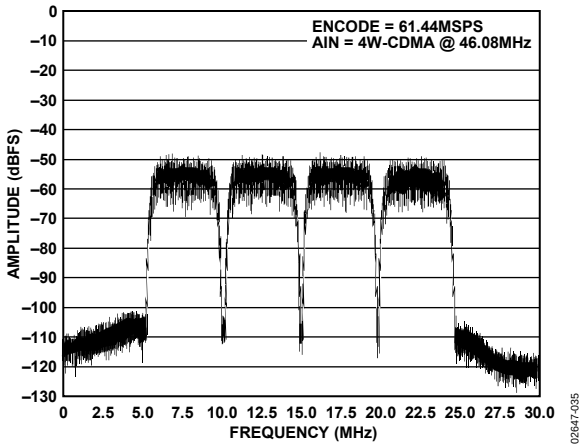

Figure 29. Four W-CDMA Carriers @ 46.08 MHz, Encode = 61.44 MSPS

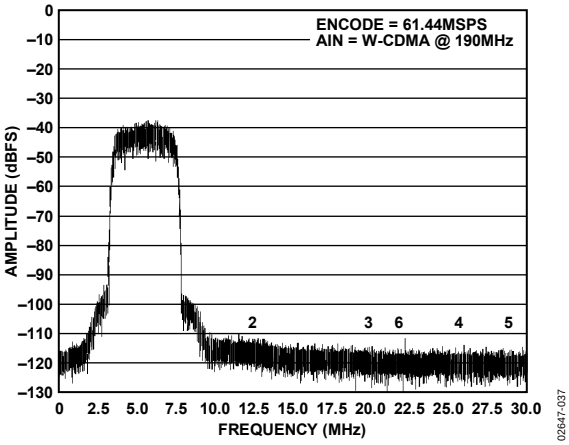

Figure 31. W-CDMA Tone @ 190 MHz, Encode = 61.44 MSPS

EQUIVALENT CIRCUITS

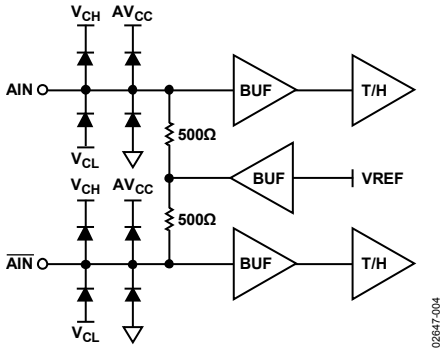

Figure 32. Analog Input Stage

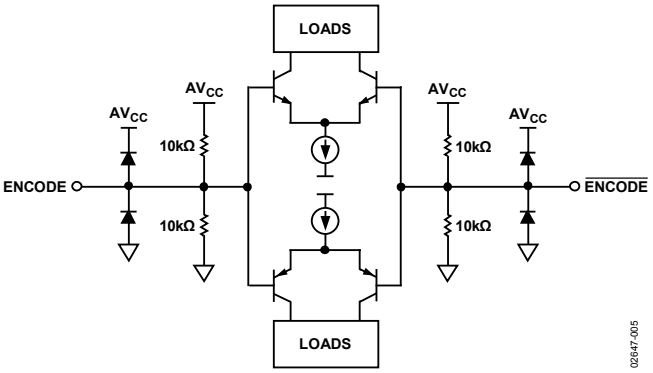

Figure 33. Encode Inputs

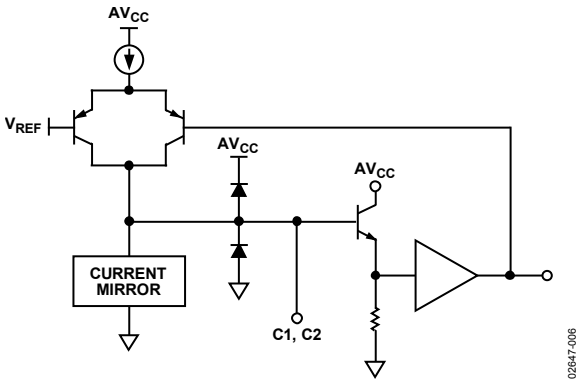

Figure 34. Compensation Pin, C1 or C2

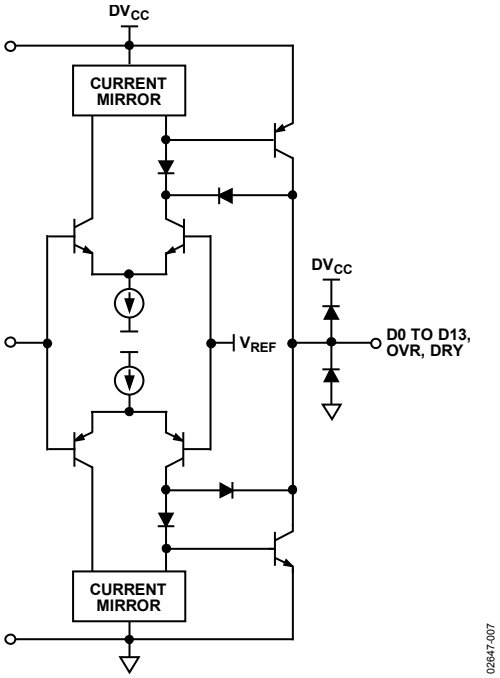

Figure 35. Digital Output Stage

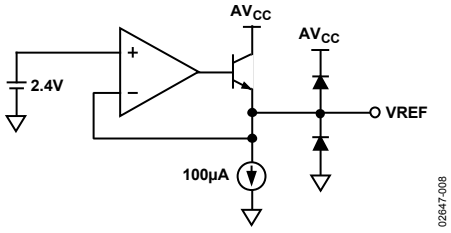

Figure 36. 2.4 V Reference

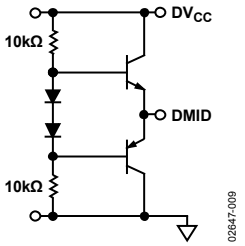

Figure 37. DMID Reference

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the encode command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. The peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. The peak-to-peak differential is computed by rotating the inputs' phase 180°and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the encode pulse should be left in a high state to achieve rated performance; pulse width low is the minimum time that the encode pulse should be left in a low state. See timing implications of changing t_{ENCH} in Table 4. At a given clock rate, these specifications define an acceptable encode duty cycle.

Full-Scale Input Power
The full-scale input power is expressed in dBm and can be calculated by using the following equation:

$$Power_{Full-Scale} = 10\log\left[\frac{\frac{V^2_{Full-Scale\,rms}}{|Z|_{Input}}}{0.001}\right]$$

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least square curve fit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Noise (for Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}$$

where:

Z is the input impedance.

FS is the full scale of the device for the frequency in question.

SNR is the value for the particular input level.

Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal noise and quantization noise.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio (PSSR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Power Supply Rise Time
The time from when the dc supply is initiated until the supply output reaches the minimum specified operating voltage for the ADC. The dc level is measured at the supply pin(s) of the ADC.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (that is, degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product, reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product, and may be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics), reported in dBc.

THEORY OF OPERATION

The AD6645 ADC employs a three-stage subrange architecture. This design approach achieves the required accuracy and speed while maintaining low power and small die size.

As shown in the functional block diagram (see Figure 1), the AD6645 has complementary analog input pins, AIN and $\overline{\text{AIN}}$. Each analog input is centered at 2.4 V and should swing ±0.55 V around this reference (see Figure 32). Because AIN and $\overline{\text{AIN}}$ are 180° out of phase, the differential analog input signal is 2.2 V p-p.

Both analog inputs are buffered prior to the first track-and-hold, TH1. The high state of the encode pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives a 5-bit digital-to-analog converter, DAC1. DAC1 requires 14 bits of precision that is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residual signal is applied to a second conversion stage consisting of a 5-bit ADC2, a 5-bit DAC2, and a pipeline TH4. The second DAC requires 10 bits of precision, which is met by the process with no trim. The input to TH5 is a second residual signal generated by subtracting the quantized output of DAC2 from the first residual signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as twos complement.

APPLYING THE AD6645

Encoding the AD6645

The AD6645 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 70 MHz analog input signals when using a high jitter clock source. See the AN-501 application note, *Aperture Uncertainty and ADC System Performance*, for complete details.

For optimum performance, the AD6645 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 38 shows one preferred method for clocking the AD6645. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit excessive amplitude swings from the clock into the AD6645 to approximately 0.8 V p-p differential. This helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD6645 and limits the noise presented to the encode inputs.

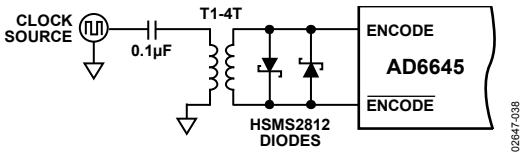

Figure 38. Crystal Clock Oscillator, Differential Encode

If a low jitter clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins, as shown in Figure 39. The MC100EL16 (or same family) from ON Semiconductor offers excellent jitter performance.

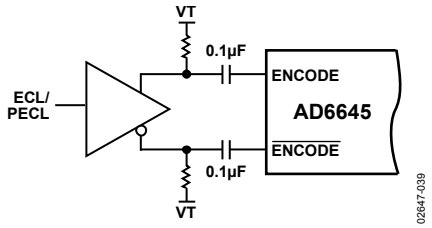

Figure 39. Differential ECL for Encode

Driving the Analog Inputs

As with most new high speed, high dynamic range ADCs, the analog input to the AD6645 is differential. Differential inputs improve on-chip performance as signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even-order harmonics. There are also benefits at the PCB level. First, differential inputs have high common-mode rejection of stray signals, such as ground and power noise. Second, they provide good rejection of common-mode signals, such as local oscillator feedthrough.

The AD6645 analog input voltage range is offset from ground by 2.4 V. Each analog input connects through a 500 Ω resistor to the 2.4 V bias voltage and to the input of a differential buffer (see Figure 32). The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6645 should be ac-coupled to the input pins. Because the differential input impedance of the AD6645 is 1 kΩ, the analog input power requirement is only −2 dBm, simplifying the driver amplifier in many cases. To take full advantage of this high input impedance, a 20:1 RF transformer is required. This is a large ratio and can result in unsatisfactory performance. In this case, a lower step-up ratio can be used. The recommended method for driving the differential analog input of the AD6645 is to use a 4:1 RF transformer. For example, if R_T is set to 60.4 Ω and R_S is set to 25 Ω, along with a 4:1 impedance ratio transformer, the input would match to a 50 Ω source with a full-scale drive of 4.8 dBm. Series resistors (R_S) on the secondary side of the transformer should be used to isolate the transformer from the A/D.

This limits the amount of dynamic current from the A/D flowing back into the secondary of the transformer. The 50 Ω impedance matching can also be incorporated on the secondary side of the transformer, as shown in the evaluation board schematic (see Figure 43).

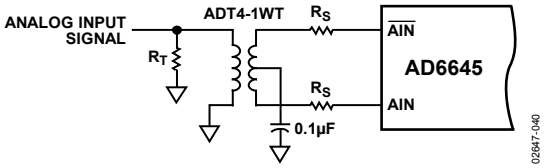

Figure 40. Transformer-Coupled Analog Input Circuit

In applications where dc coupling is required, a differential output op amp, such as the AD8138, can be used to drive the AD6645 (see Figure 41). The AD8138 op amp provides single-ended-to-differential conversion, which reduces overall system cost and minimizes layout requirements.

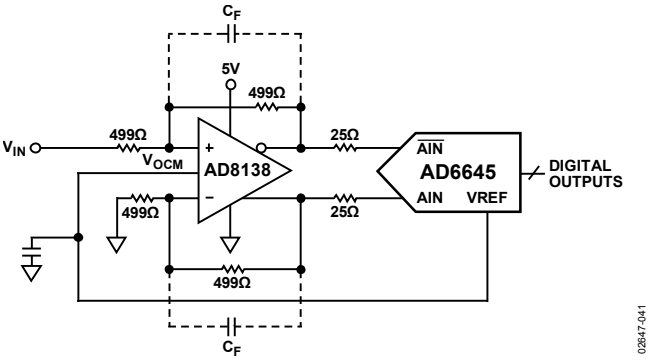

Figure 41. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. The use of linear dc supplies with rise times of <45 ms is highly recommended. Switching supplies tend to have radiated components that can be received by the AD6645. Decouple each of the power supply pins as close to the package as possible using 0.1 µF chip capacitors.

The AD6645 has separate digital and analog power supply pins. The analog supplies are AV_{CC} and the digital supply pins are DV_{CC}. Although analog and digital supplies can be tied together, the best performance is achieved when the supplies are separate because the fast digital output swings can couple switching currents back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD6645 is specified for DV_{CC} = 3.3 V, a common supply for digital ASICs.

Digital Outputs

Care must be taken when designing the data receivers for the AD6645. It is recommended that the digital outputs drive a series resistor followed by a gate, such as the 74LCX574.

To minimize capacitive loading, there should be only one gate on each output pin. An example of this is shown in the evaluation board schematic of Figure 43. The digital outputs of the AD6645 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA (10 pF × 1 V ÷ 1 ns) of dynamic current per bit flow in or out of the device. A full-scale transition can cause up to 140 mA (14 bits × 10 mA/bit) of current to flow through the output stages. Place the series resistors as close to the AD6645 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and DV_{CC}. Standard TTL gates should be avoided because they can add appreciably to the dynamic switching currents of the AD6645. Note that extra capacitive loading increases output timing and invalidates timing specifications. Digital output timing is guaranteed for output loads up to 10 pF. Digital output states for given analog input levels are shown in Table 8.

Grounding

For optimum performance, it is highly recommended that a common ground be used between the analog and digital power planes. The primary concern with splitting grounds is that dynamic currents may be forced to travel significant distances in the system before recombining back at the common source ground. This can result in a large, undesirable ground loop. The most common place for this to occur is on the digital outputs of the ADC. Ground loops can contribute to digital noise being coupled back onto the ADC front end. This can manifest itself as either harmonic spurs, or very high-order spurious products that can cause excessive spikes on the noise floor. This noise coupling is less likely to occur at lower clock speeds because the digital noise has more time to settle between samples. In general, splitting the analog and digital grounds can frequently contribute to undesirable EMI-RFI and should, therefore, be avoided.

Conversely, if not properly implemented, common grounding can actually impose additional noise issues because the digital ground currents ride on top of the analog ground currents in close proximity to the ADC input. To further minimize the potential for noise coupling, it is highly recommended that multiple ground return traces/vias be placed such that the digital output currents do not flow back toward the analog front end but are routed quickly away from the ADC. This does not require a split in the ground plane and can be accomplished by simply placing substantial ground connections directly back to the supply at a point between the analog front end and the digital outputs. In addition, the judicious use of ceramic chip capacitors between the power supply and ground planes helps to suppress digital noise. The layout should incorporate enough bulk capacitance to supply the peak current requirements during switching periods.

LAYOUT INFORMATION

The schematic of the evaluation board (see Figure 43) represents a typical implementation of the AD6645. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6645 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6645, minimal capacitive loading should be placed on these outputs. It is recommended that a fanout of only one gate should be used for all AD6645 digital outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

Table 8. Twos Complement Output Coding

AIN Level	$\overline{\text{AIN}}$ Level	Output State	Output Code
VREF + 0.55 V	VREF − 0.55 V	Positive FS	01 1111 1111 1111
VREF	VREF	Midscale	00 … 0/11 … 1
VREF − 0.55 V	VREF + 0.55 V	Negative FS	10 0000 0000 0000

JITTER CONSIDERATIONS

The SNR for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms: jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$SNR = 1.76 - 20\log\left[\left(2\pi \times f_{ANALOG} \times t_{jrms}\right)^2 + \left(\frac{1+\varepsilon}{2^n}\right)^2 + \left(\frac{2\times\sqrt{2}\times V_{NOISE\,rms}}{2^n}\right)^2\right]^{1/2}$$

where:

f_{ANALOG} is the analog input frequency.

$t_{j\,rms}$ is the rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ε is the average DNL of the ADC (typically 0.41 LSB).

n is the number of bits in the ADC.

$V_{NOISE\,rms}$ is the voltage rms thermal noise that refers to the analog input of the ADC (typically 0.9 LSB rms).

For a 14-bit ADC, such as the AD6645, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. Figure 42 shows a family of curves that demonstrate the expected SNR performance of the AD6645 as jitter increases. The chart is derived from the preceding equation.

For a complete discussion of aperture jitter, see the AN-756 application note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*. The AN-756 application note can be found on www.analog.com.

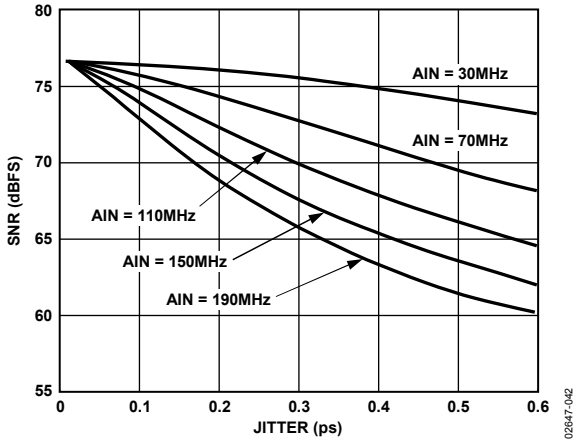

Figure 42. SNR vs. Jitter

Table 9. AD6645/PCB Bill of Materials

Quantity 80 MSPS	Quantity 105 MSPS	Reference ID	Description	Manufacturer	Supplier Part No.
1	1	PCB	Printed circuit board, AD6645 engineering evaluation board	PCSM	6645EE01D REV D
4	4	C1, C2, C31, C38	Capacitor, tantalum, SMT BCAPTAJC, 10 µF, 16 V, 10%	Kemet	T491C106K016AS
8	8	C3, C7 to C10, C16, C30[1], C32	Capacitor, ceramic, SMT 0508, 0.1 µF, 16 V, 10%	Presidio Components	0508X7R104K16VP3
9	9	C4, C15, C22 to C26, C29, (C33)[2, 3], (C34)[2, 3], C39	Capacitor, ceramic, SMT 0805, 0.1 µF, 25 V, 10%	Panasonic	ECJ-2VB1E104K
0	0	(C5, C6)[2, 3]	Capacitor, ceramic, SMT 0805, 0.01 µF, 50 V, 10%	Panasonic	ECJ-2YB1H103K
10	10	C11 to C14, C17 to C21, C40	Capacitor, ceramic, SMT 0508, 0.01 µF, 50 V, 0.2%	Presidio Components	0508X7R103M2P3
0	0	(C27, C28)[2]	Capacitor, ceramic, SMT 0805, limits amp bandwidth as warranted		
1	1	CR1[3]	Diode, dual Schottky HSMS2812, SOT-23, 30 V, 20 mA	Panasonic	MA716-(TX)
1	1	E1	Install jumper wire (across OPT_LAT and BUFLAT)		
5	5	F1 to F5	EMI suppression ferrite chip, SMT 0805	Steward	HZ0805E601R-00
1	1	J1	Header, 6-pin, pin strip, 5 mm pitch	Wieland	Z5.530.0625.0
1	1	J1	Pin strip, 6-pin, 5 mm pitch	Wieland	25.602.2653.0
1	1	J2	Header, 40-pin, male, right angle	Samtec	TSW-120-08-T-D-RA
2	2	(J3)[2], J4, J5	Connector, gold, female, coax., SMA, vertical	Johnson Components	142-0701-201
1	1	L1	Inductor, SMT, 1008-ct package, 4.7 nH	Coilcraft	1008CT-040X-J
0	0	(R1)[2, 3]	Resistor, thick film, SMT 0402, 100 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1000
0	0	(R2)[2]	Resistor, thick film, SMT 1206, 60.4 Ω, 1/4 W, 1%	Panasonic	ERJ-8ENF60R4V
2	2	(R3 to R5)[1, 2], (R8)[1, 2], R9, R10	Resistor, thick film, SMT 0805, 500 Ω, 1/8 W, 1%	Panasonic	ERJ-6ENF4990V
2	2	R6, R7	Resistor, thick film, SMT 0805, 25.5 Ω, 1/8 W, 1%	Panasonic	ERJ-6ENF25R5V
0	0	(R11)[2, 3], (R13)[2, 3]	Resistor, thick film, SMT 0805, 66.5 Ω, 1/8 W, 1%	Panasonic	ERJ-6ENF66R5V
0	0	(R12)[2, 3], (R14)[2, 3]	Resistor, thick film, SMT 0805, 100 Ω, 1/8W, 1%	Panasonic	ERJ-6ENF1000V
1	1	R15[1]	Resistor, thick film, SMT 0402, 178 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF1780X
1	1	R35	Resistor, thick film, SMT 0805, 49.9 Ω, 1/8 W, 1%	Panasonic	ERJ-6ENF49R9V
4	4	RN1 to RN4	Resistor array, SMT 0402; 100 Ω; 8 ISO RES.,1/4 W; 5%	Panasonic	EXB2HV101JV
2	2	T2[3], T3[1]	Transformer, ADT4-1WT, CD542, 2 MHz to 775 MHz	Mini-Circuits	ADT4-1WT
1	0	U1	IC, 14-bit, 80 MSPS ADC	Analog Devices	AD6645ASQ/ASV-80
0	1	U1	IC, 14-bit, 105 MSPS ADC	Analog Devices	AD6645ASQ/ASV-105
2	2	U2, U7	IC, SOIC-20, Octal D-type flip-flop	Fairchild	74LCX574WM
0	0	(U3)[1, 2]	IC, SOIC-8, low distortion differential ADC driver	Analog Devices	AD8138AR
2	2	U4, U6	IC, SOT-23, tiny logic UHS 2 input OR gate	Fairchild	NC7SZ32

Quantity 80 MSPS	Quantity 105 MSPS	Reference ID	Description	Manufacturer	Supplier Part No.
0	0	(U8)[2, 3]	IC, SOIC-8, differential receiver	Motorola	MC100LVEL16
1	0	Y1	Clock oscillator, 80 MHz	CTS Reeves	MXO45-80
4	4	Y1	Pin sockets, closed end	AMP/Tyco Electronics	5-330808-3
4	4		Circuit board support	Richco, Inc.	CBSB-14-01

[1] AC-coupled AIN is standard: R3, R4, R5, R8, and U3 are not installed. If dc-coupled AIN is required, C30, R15, and T3 are not installed.
[2] Reference designators in parentheses are not installed on standard units.
[3] AC-coupled encode is standard: C5, C6, C33, C34, R1, R11 to R14, and U8 are not installed. If PECL encode is required, CR1 and T2 are not installed.

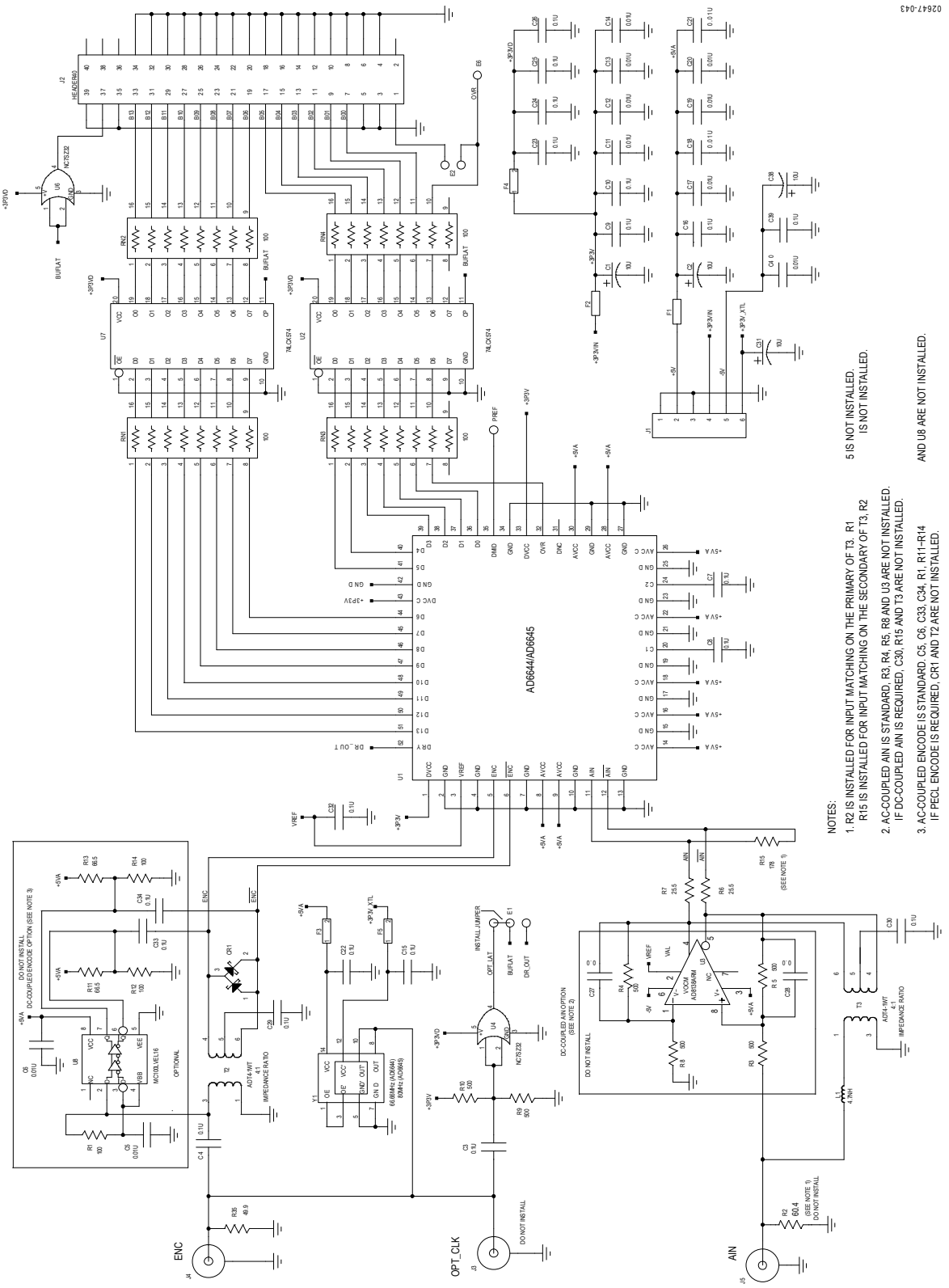

Figure 43. Evaluation Board Schematic

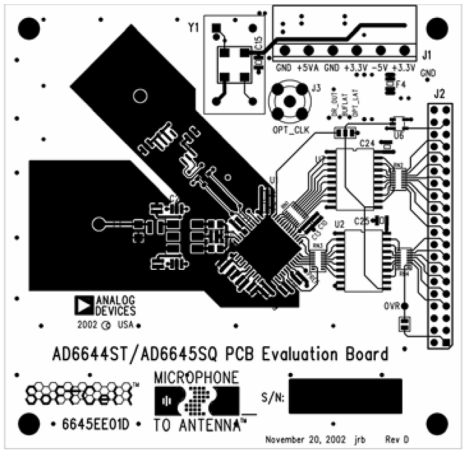

Figure 44. Top Signal Level

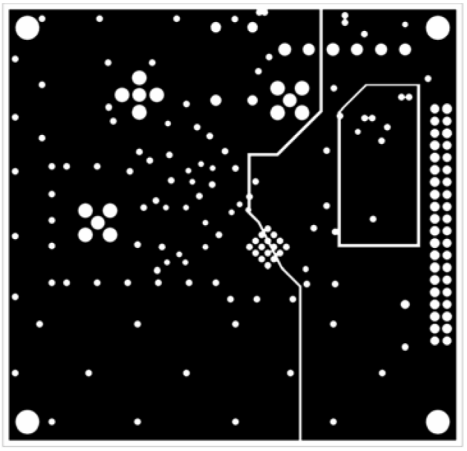

Figure 45. 5.0 V Plane Layer 3 and 3.3 V Plane Layer 4

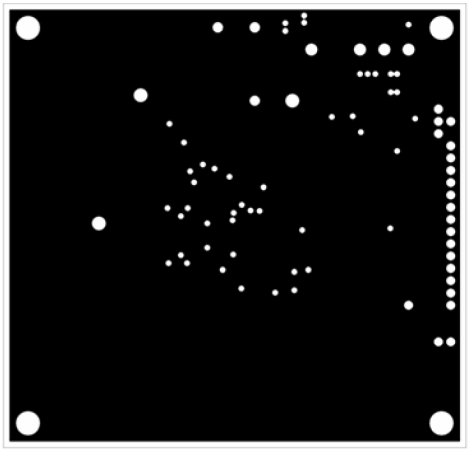

Figure 46. Ground Plane Layer 2 and Ground Plane Layer 5

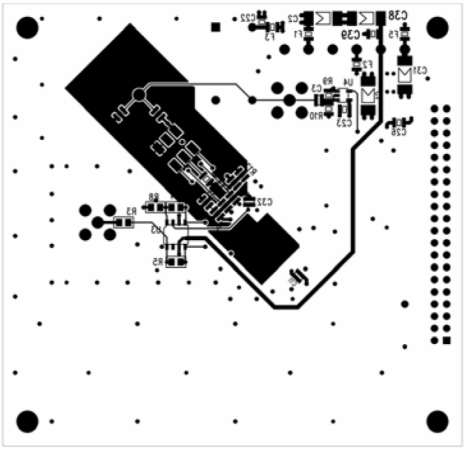

Figure 47. Bottom Signal Layer

OUTLINE DIMENSIONS

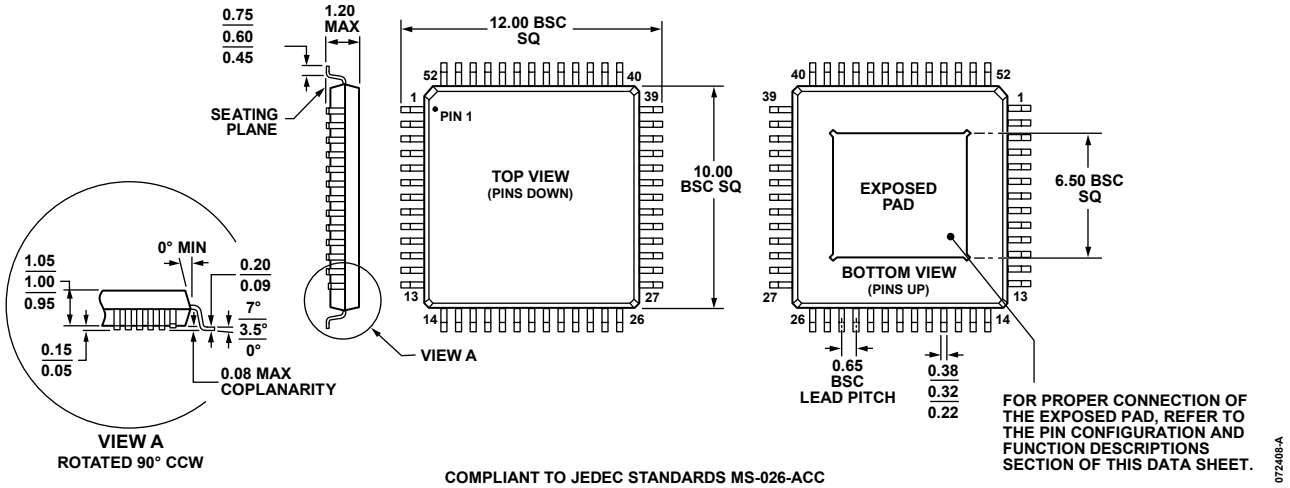

Figure 48. 52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-52-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6645ASVZ-80	−40°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-1
AD6645ASVZ-105	−10°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-1
AD6645-105/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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AD6645ASVZ-80 AD6645ASVZ-105