8 Channel Signal Retimer for 8.0Gps, 5.0Gbps and 2.5Gbps PCIe®

89HT0808P
Product Brief

Device Overview

The 89HT0808P (T0808P) is a Signal Retimer/Conditioner used to improve signal integrity for enhancing system performance and reliability across long PCB traces or cables. It removes both random and deterministic jitter from the input signal eliminating inter-symbol interference, and resets the output jitter budget. It provides eight differential, 8Gbps PCIe Express® 3.0 channels, supporting up to 4 full lanes. The Retimer also fully supports PCIe Express 5Gbps and 2.5Gbps features. The T0808P is targeted to meet the high-performance needs of PCIe® Gen 3/2/1 applications.

Applications

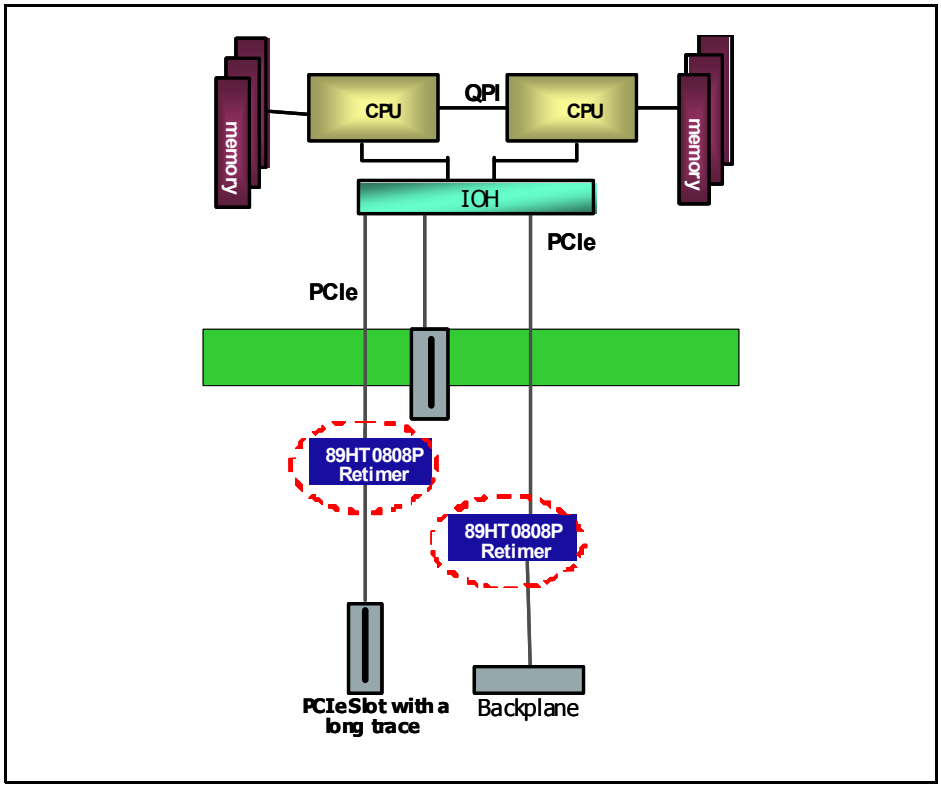
- Computing and Storage
- Consumer Electronics and Communications

Features

- **High Performance Retimer**
  - Eliminates random input jitter
  - Eliminates deterministic ISI jitter
  - Compensates for PCB trace and cable attenuations
  - Performance and power tunable for each data rate
  - Wide swing, transmit driver offers up to 8dB of transmit de-emphasis to meet the needs of the most challenging of backplanes
  - Multi-stage equalizer: CTLE and 5 tap DFE
  - Fast acquisition PLL for L0s exit
  - SERDES Rx eye generation (on-chip)
- **PCIe Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - PCI Express Base Specification 2.1 compliant
- **Power Management**
  - Low power
  - Supports the following optional PCI Express features
    - L0s ASPM
    - L1 ASPM
- **Hot Plug Support**
- **SerDes Power Savings**
  - Supports low swing (half-swing) SerDes operation
  - SerDes associated with unused lanes are placed in a low power state automatically
- **Link Configurability**
  - Links can be configured with 1x4, 1x1, 2x1
  - Automatic per port link width negotiation (e.g., a x4 port can link train to x4 or x1)
  - Per-lane SerDes configuration
    - De-emphasis, receive equalization, drive strength
- **Clocking**
  - Uses standard 100 MHz PCIe reference clock
  - SSCLK (Spread Spectrum Clocking) supported with common clock configuration
  - Non-SSCLK supported with common and non-common clock configuration
- **I^2C Interface**
  - Dedicated master interface
    - External EEPROM configuration loading
  - Dedicated slave interface
    - Configuration loading
    - Writing new or initial image into external EEPROM
    - Expose internal global CSR space to system controller
- **Reliability, Availability and Serviceability (RAS)**
  - Physical layer error checking and accounting
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
- **Test and Debug**
  - Per link/lane error diagnostic registers
  - All registers accessible from I^2C or JTAG port
  - SerDes test modes
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
  - Several loopback modes
- **Packaged in a 9x9mm, 100-pin BGA, 0.8mm ball spacing**

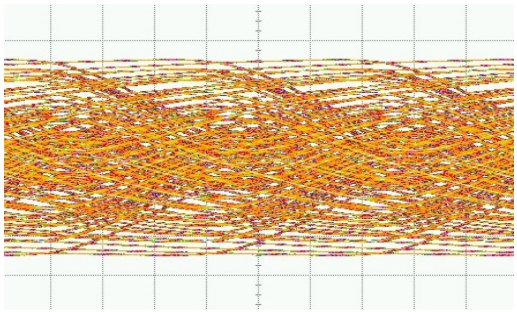
Applications

IDT's Retimer products fit into server, storage, and blade products.

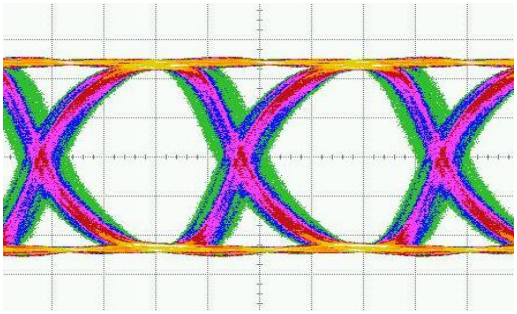


Improving Signal Integrity with IDT Retimers

No Retimer



With IDT Retimer



Example Eye diagram FR4 and PRBS patterns

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