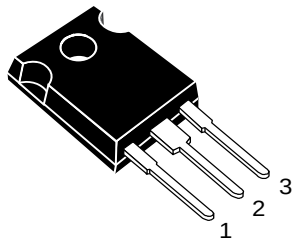
STW48N60M2

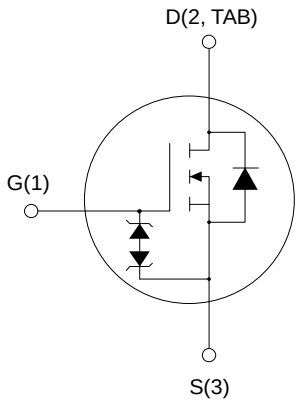
N-channel 600 V, 0.06 Ω typ., 42 A MDmesh™ M2 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D
STW48N60M2	650 V	0.07 Ω	42 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW48N60M2	48N60M2	TO-247	Tube

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	42	A
I_D	Drain current (continuous) at T_C = 100 °C	26	A
I_{DM} (1)	Drain current (pulsed)	168	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)$I_{SD} \leq 42$ A, di/dt ≤ 400 A/µs; $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V

(3)$V_{DS} \leq 480$ V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	0.42	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax.}$)	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$; V_{DD} = 50 V)	1	J

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0, V_{DS}= 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 21 A		0.06	0.07	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 100 V, f = 1 MHz	-	3060	-	pF
C_{oss}	Output capacitance		-	143	-	pF
C_{rss}	Reverse transfer capacitance		-	4.3	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	630	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0	-	4.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 42 A, V_{GS} = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	70	-	nC
Q_{gs}	Gate-source charge		-	10.5	-	nC
Q_{gd}	Gate-drain charge		-	31	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 21 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	18.5	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off-delay time		-	13	-	ns
t_f	Fall time		-	119	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		42	A
I_{SDM}(1)	Source-drain current (pulsed)		-		168	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0, I_{SD} = 21 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 42 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 17: "Unclamped inductive load test circuit"*)	-	487		ns
Q_{rr}	Reverse recovery charge		-	9.1		µC
I_{RRM}	Reverse recovery current		-	37.5		A
t_{rr}	Reverse recovery time	I_{SD} = 42 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Unclamped inductive load test circuit"*)	-	605		ns
Q_{rr}	Reverse recovery charge		-	12.5		µC
I_{RRM}	Reverse recovery current		-	41.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

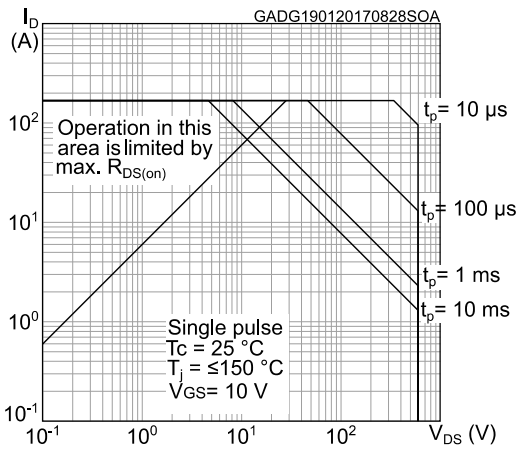


Figure 3: Thermal impedance

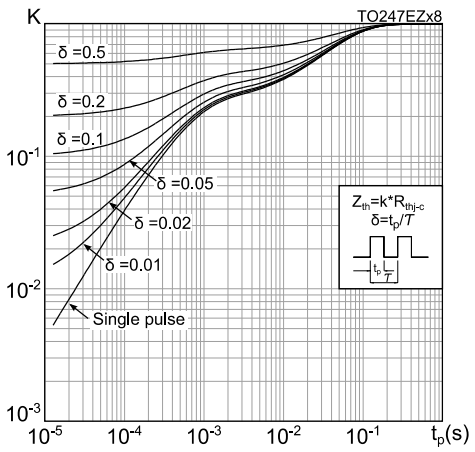


Figure 4: Output characteristics

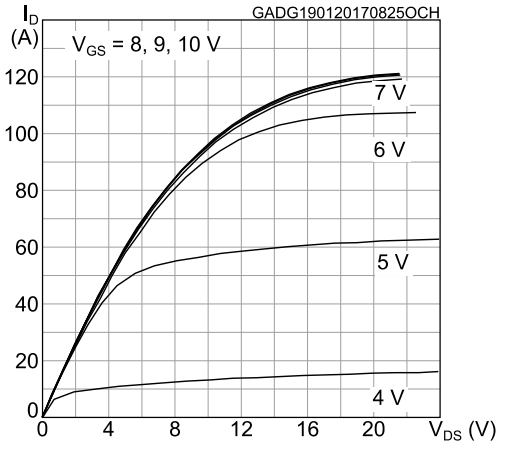


Figure 5: Transfer characteristics

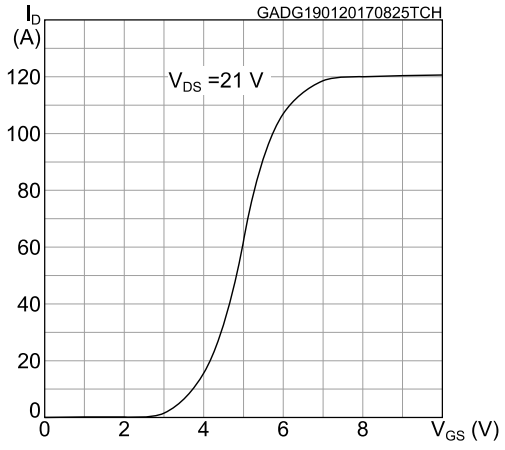


Figure 6: Gate charge vs gate-source voltage

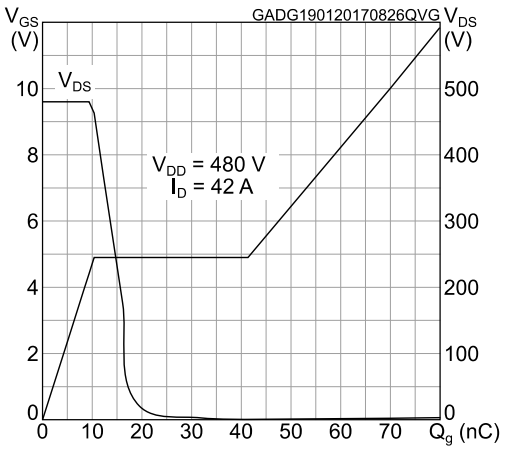


Figure 7: Static drain-source on-resistance

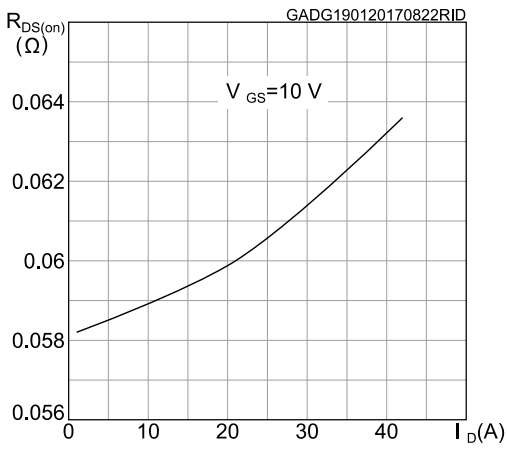


Figure 8: Capacitance variations

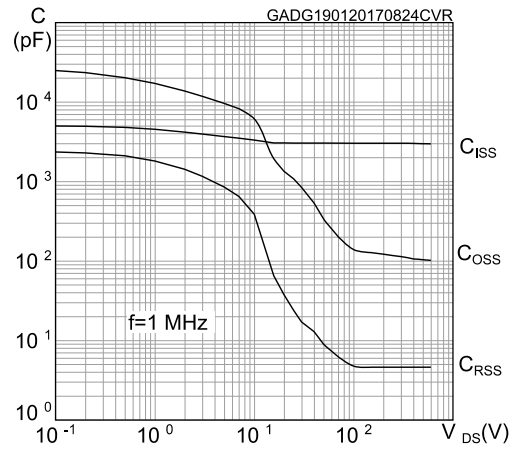


Figure 9: Output capacitance stored energy

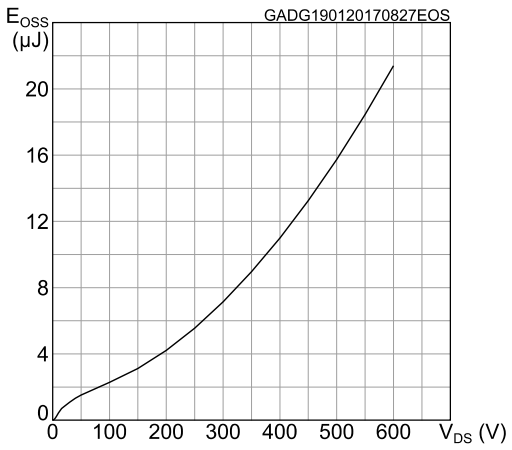


Figure 10: Normalized gate threshold voltage vs temperature

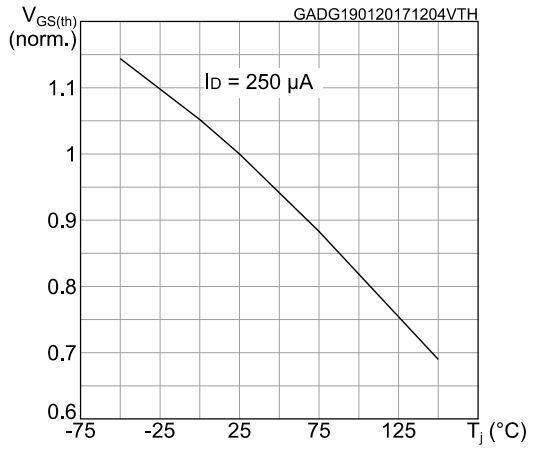


Figure 11: Normalized on-resistance vs temperature

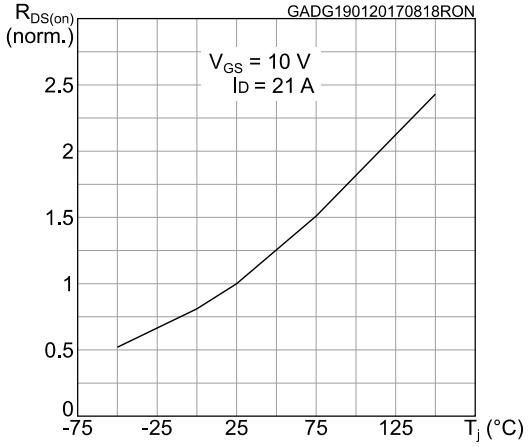


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

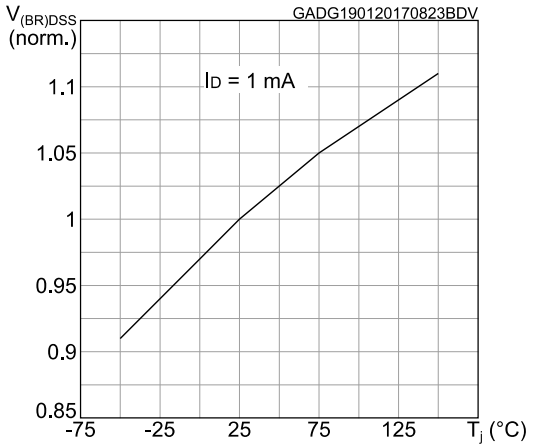
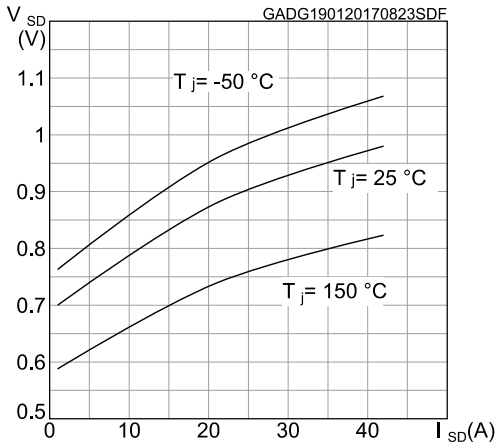


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

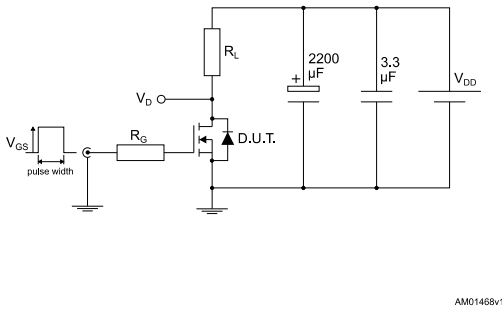


Figure 15: Test circuit for gate charge behavior

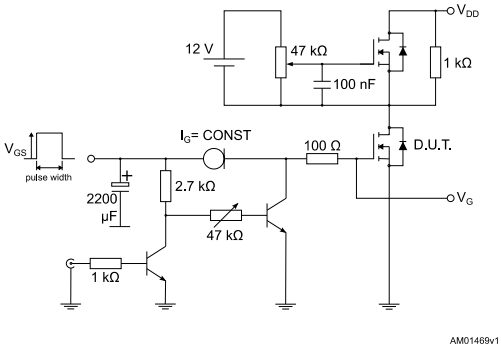


Figure 16: Test circuit for inductive load switching and diode recovery times

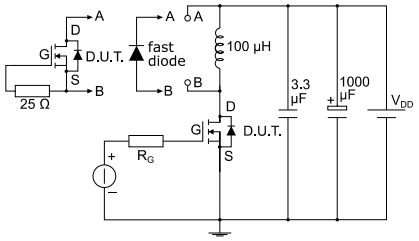


Figure 17: Unclamped inductive load test circuit

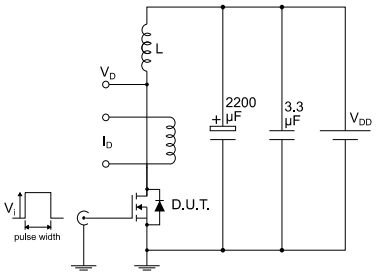


Figure 18: Unclamped inductive waveform

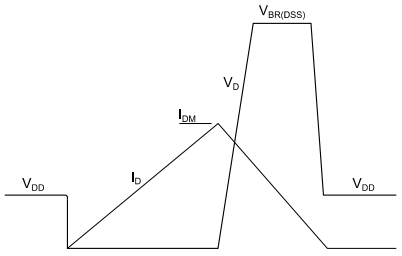
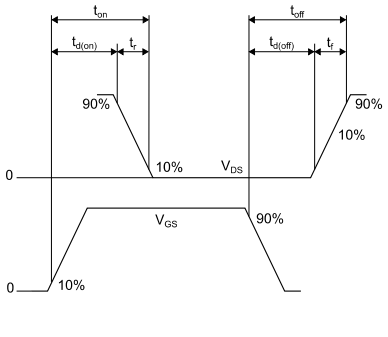


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

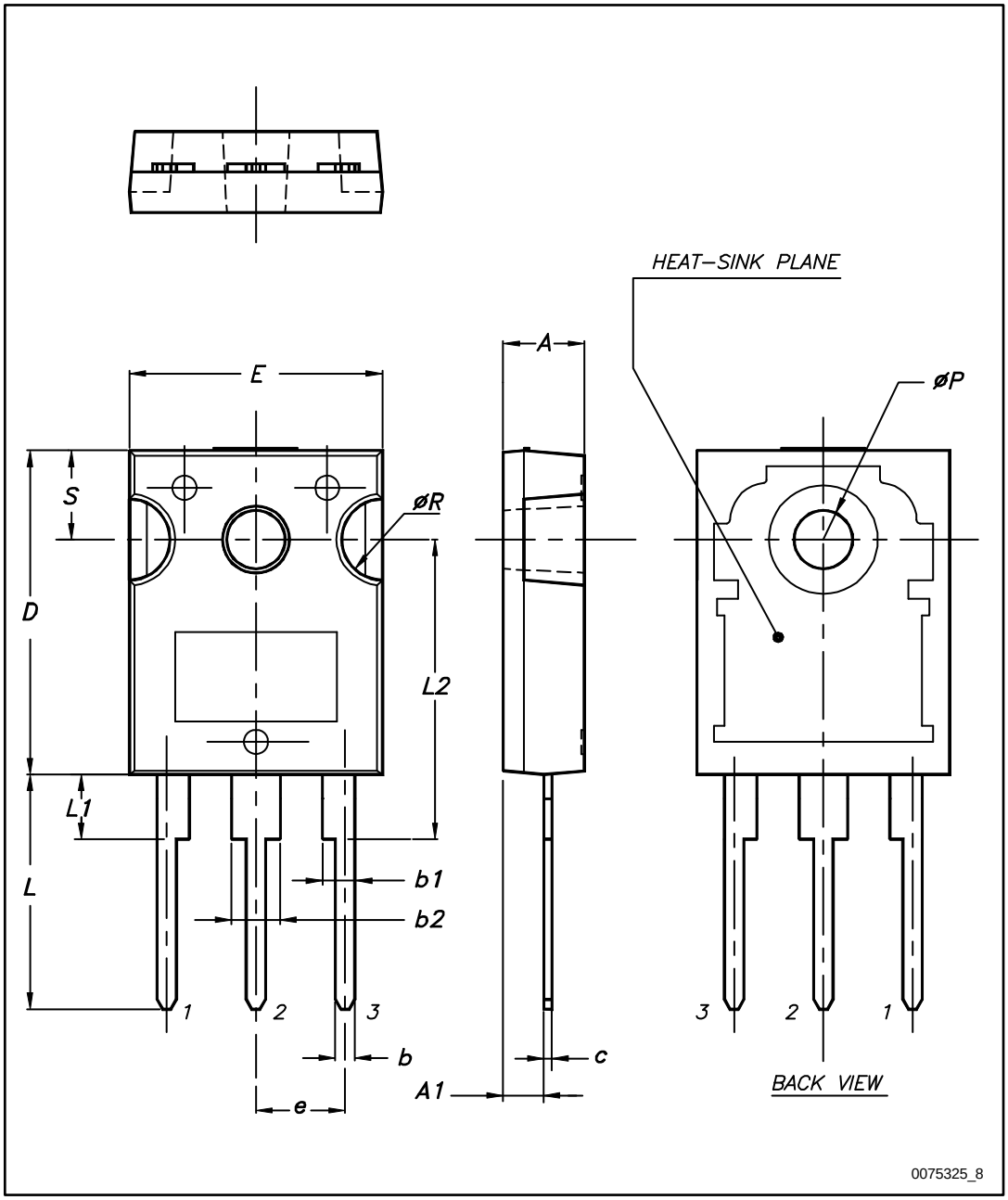


Table 9: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
09-Jun-2014	1	First release.
01-Sep-2014	2	Document status promoted from preliminary to production data. Added *Section 2.1: "Electrical characteristics curves"*. Minor text changes.
19-Jan-2017	3	Updated *Table 2: "Absolute maximum ratings"*, *Table 4: "Avalanche characteristics"*, *Table 5: "On /off-states"* and *Table 7: "Switching times"*. Updated *Section 2.1: "Electrical characteristics (curves)"*.

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