LM4879 Boomer® Audio Power Amplifier Series 1.1 Watt Audio Power Amplifier

Check for Samples: LM4879, LM4879MMBD, LM4879SDBD

FEATURES

- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Unity Gain Stable**
- **Ultra Low Current Shutdown Mode**
- **Fast Turn On: 80ms (typ), 110ms (max) with 1.0µF Capacitor**
- **BTL Output Can Drive Capacitive Loads up to 100pF**
- **Advanced Pop and Click Circuitry Eliminates Noises During Turn-On and Turn-Off Transitions**
- **2.2V - 5.0V Operation**
- **Available in Space-Saving DSBGA, WSON, and VSSOP Packages**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable electronic devices**

KEY SPECIFICATIONS

- **PSRR: 5V, 3V at 217Hz: 62dB (typ)**
- **Power Output at 5V, 1%THD+N: 1.1W (typ)**
- **Power Output at 3V, 1%THD+N: 350mW (typ)**
- **Shutdown Current: 0.1µA (typ)**

DESCRIPTION

The LM4879 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer™ audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4879 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for lower-power portable applications where minimal space and power consumption are primary requirements.

The LM4879 features a low-power consumption global shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4879 features an internal thermal shutdown protection mechanism.

The LM4879 contains advanced pop and click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4879 is unity-gain stable and can be configured by external gain-setting resistors.

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TYPICAL APPLICATION

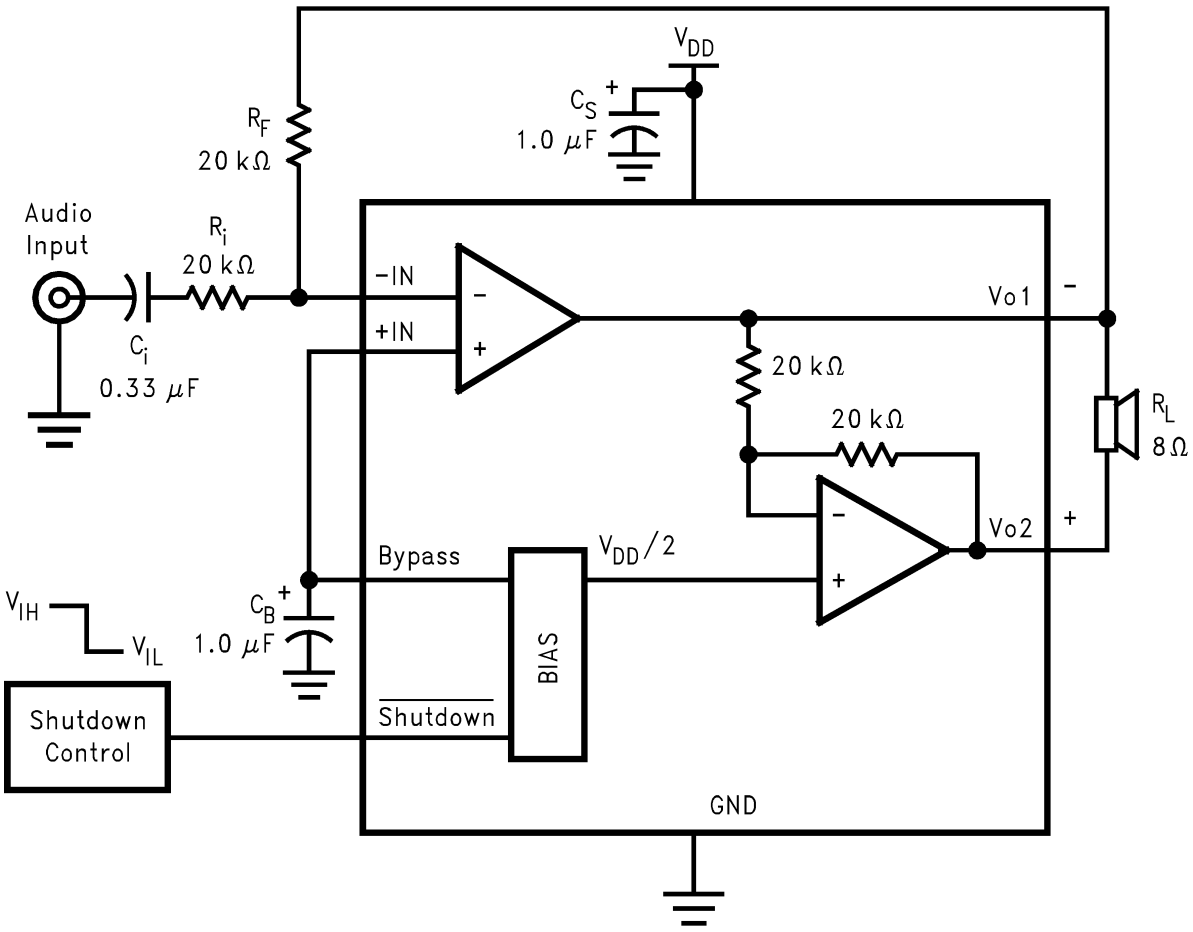

Figure 1. Typical Audio Amplifier Application Circuit

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CONNECTION DIAGRAMS

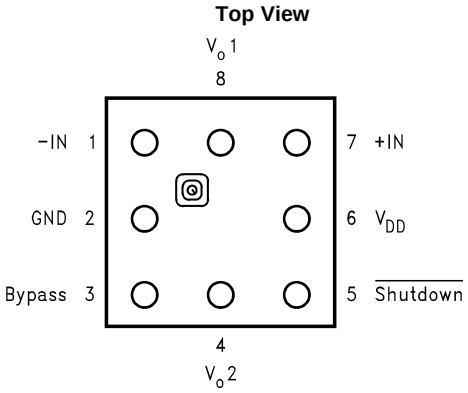

Figure 2. 8 Bump DSBGA Package
See Package Number YPB0008

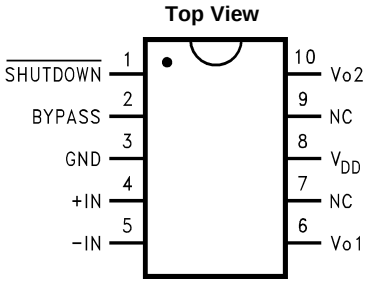

Figure 3. VSSOP Package
See Package Number DGS0010A
NC = No Connect

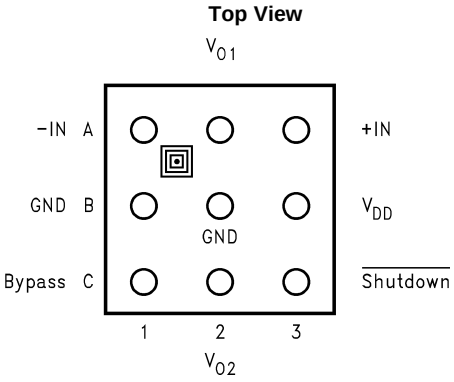

Figure 4. 9 Bump DSBGA Package
See package Number BLA09AAB

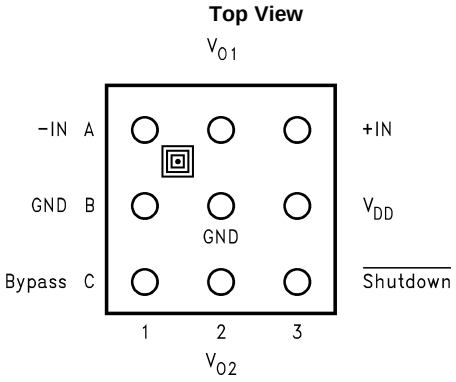

Figure 5. 9 Bump DSBGA Package
See package Number YZR0009AAA

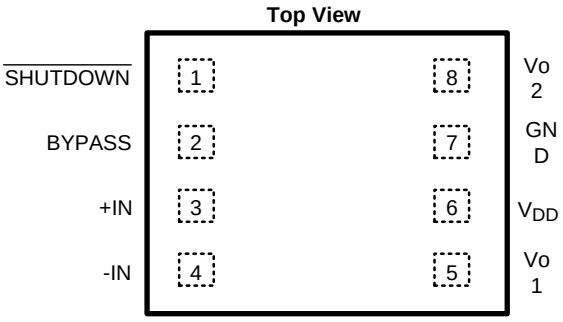

Figure 6. WSON Package
See Package Number NGT0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage(3)		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(4)(5)		Internally Limited
ESD Susceptibility(6)		2000V
ESD Susceptibility(7)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (YPB0008)	220°C/W(8)
	θ_{JA} (NGT0008A)	64°C/W(9)
	θ_{JA} (YZR0009AAA)	180°C/W(8)
	θ_{JA} (BLA09AAB)	180°C/W(8)
	θ_{JC} (DGS0010A)	56°C/W
	θ_{JA} (DGS0010A)	190°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) If the product is in shutdown mode, and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will flow through the ESD protection circuits. If the source impedance limits the current to a max of 10ma, then the part will be protected. If the part is enabled when V_{DD} is above 6V, circuit performance will be curtailed or the part may be permanently damaged.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4879, see power derating curves for additional information.
(5) Maximum power dissipation (P_{DMAX}) in the device occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 2 shown in the APPLICATION INFORMATION section. It may also be obtained from the power dissipation graphs.
(6) Human body model, 100pF discharged through a 1.5kΩ resistor.
(7) Machine Model, 220pF–240pF discharged through all pins.
(8) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance.
(9) The stated θ_{JA} is achieved when the WSON package's DAP is soldered to a $4in^2$ copper heatsink plain.

OPERATING RATINGS

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

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ELECTRICAL CHARACTERISTICS V_{DD} = 5V (1)(2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4879		Units (Limits)
			Typ (3)	Limit (4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	5	10	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage		5	40	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	1.1	0.9	W (min)
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	68 (f = 1kHz) 62 (f = 217Hz)	55	dB (min)
V_{SDIH}	Shutdown High Input Voltage			1.4	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 1.0µF	80	110	ms (max)
N_{OUT}	Output Noise	A-Weighted; Measured across 8Ω BTL Input terminated with 10Ω to ground	26		μV_{RMS}

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

ELECTRICAL CHARACTERISTICS V_{DD} = 3.0V (1)(2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4879		Units (Limits)
			Typ (3)	Limit (4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	4.5	9	mA (max)
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage		5	40	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	350	320	mW
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	68 (f = 1kHz) 62 (f = 217Hz)	55	dB (min)
V_{SDIH}	Shutdown High Input Voltage			1.4	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 1.0µF	80	110	ms (max)
N_{OUT}	Output Noise	A-Weighted; Measured across 8Ω BTL Input terminated with 10Ω to ground	26		μV_{RMS}

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

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ELECTRICAL CHARACTERISTICS V_{DD} = 2.6V (1) (2)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4879		Units (Limits)
			Typ (3)	Limit (4) (5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, 8Ω BTL	3.5		mA
I_{SD}	Shutdown Current	$V_{shutdown}$ = GND	0.1		µA
V_{OS}	Output Offset Voltage		5		mV
P_o	Output Power	THD+N = 1% (max); f = 1kHz			
		R_L = 8Ω	250		mW
		R_L = 4Ω	350		
THD+N	Total Harmonic Distortion+Noise	P_o = 0.1Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 1.0µF Input terminated with 10Ω to ground	55 (f = 1kHz) 55 (f = 217Hz)		dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

EXTERNAL COMPONENTS DESCRIPTION

(See Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

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TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, PWR = 250mW

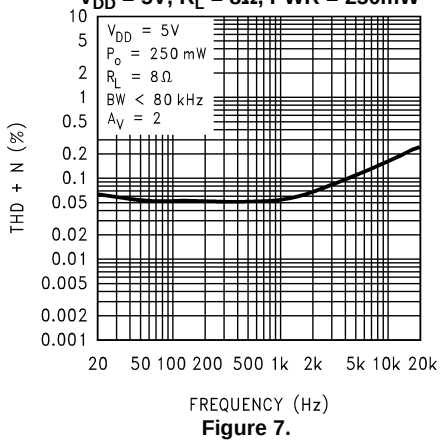

Figure 7.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, PWR = 150mW

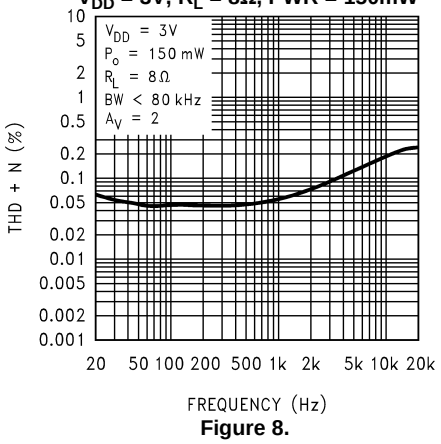

Figure 8.

THD+N vs Frequency
V_{DD} = 2.6V, R_L = 8Ω, PWR = 100mW

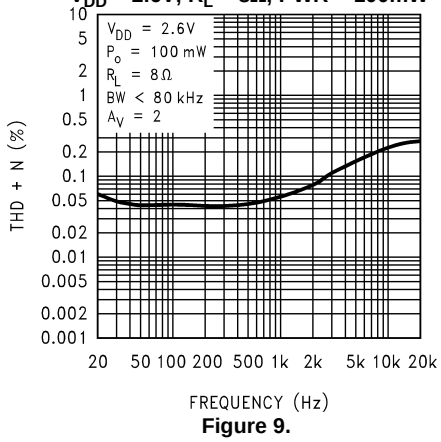

Figure 9.

THD+N vs Frequency
V_{DD} = 2.6V, R_L = 4Ω, PWR = 100mW

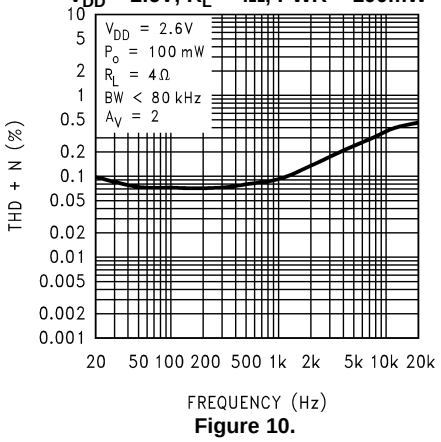

Figure 10.

THD+N vs Power Out
V_{DD} = 5V, R_L = 8Ω, f = 1kHz

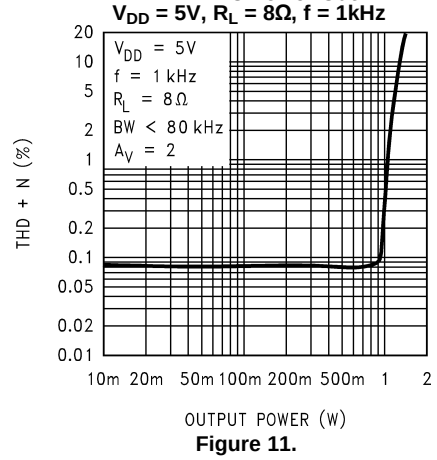

Figure 11.

THD+N vs Power Out
V_{DD} = 3V, R_L = 8Ω, f = 1kHz

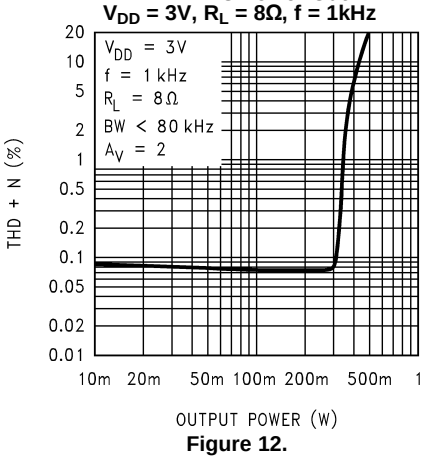

Figure 12.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Power Out
V_{DD} = 2.6V, R_L = 8Ω, f = 1kHz

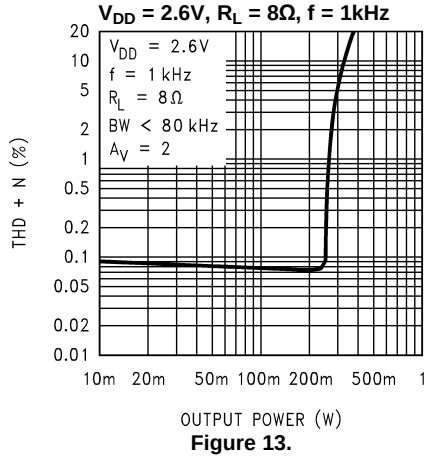

Figure 13.

THD+N vs Power Out
V_{DD} = 2.6V, R_L = 4Ω, f = 1kHz

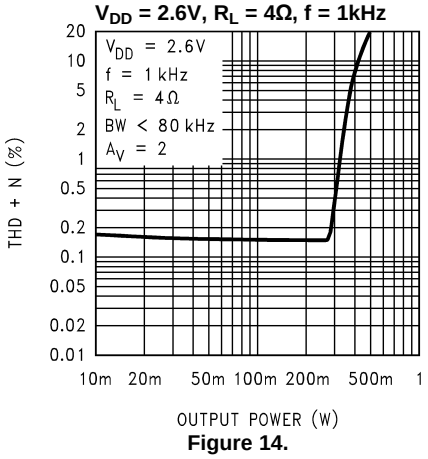

Figure 14.

Power Supply Rejection Ratio
V_{DD} = 5V

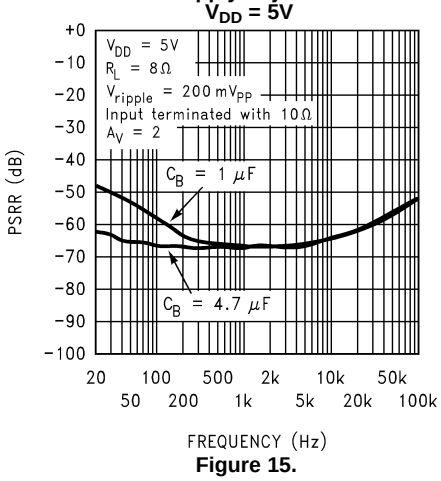

Figure 15.

Power Supply Rejection Ratio
V_{DD} = 3V

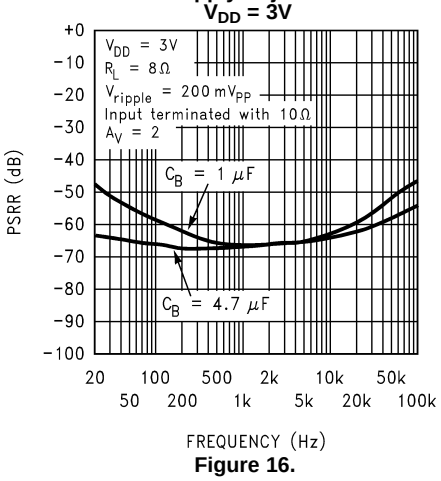

Figure 16.

Power Supply Rejection Ratio
V_{DD} = 2.6V

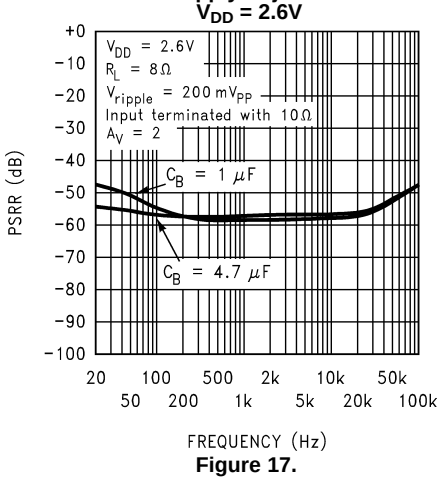

Figure 17.

Power Dissipation
vs Output Power
V_{DD} = 5V

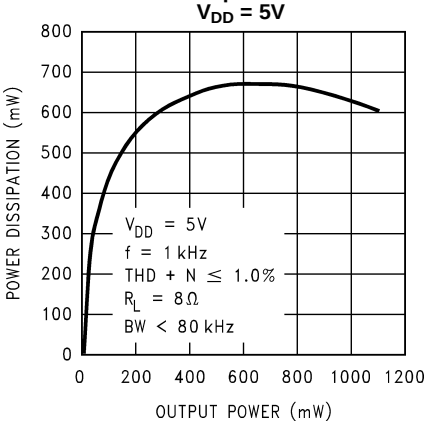

Figure 18.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Dissipation vs Output Power V_{DD} = 3V

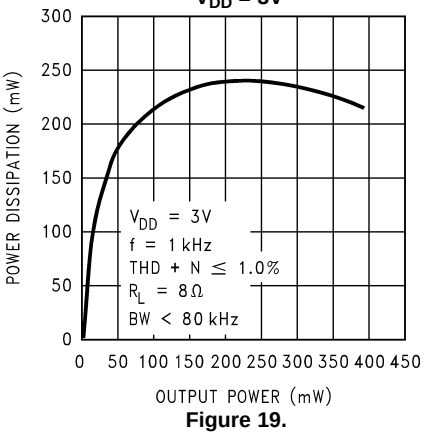

Figure 19.

Power Dissipation vs Output Power V_{DD} = 2.6V

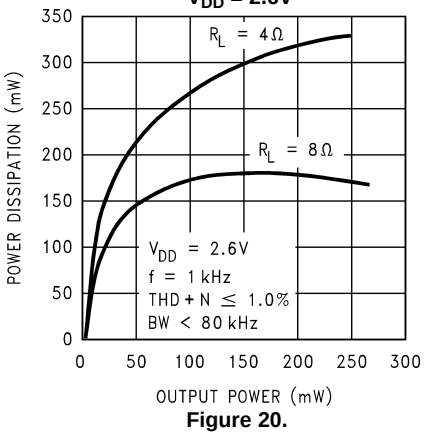

Figure 20.

Power Dissipation vs Output Power (LLP Package) V_{DD} = 5V

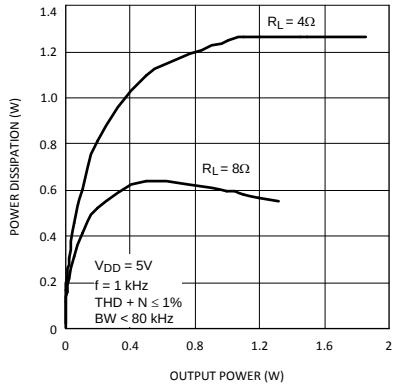

Figure 21.

Power Derating - MSOP P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω

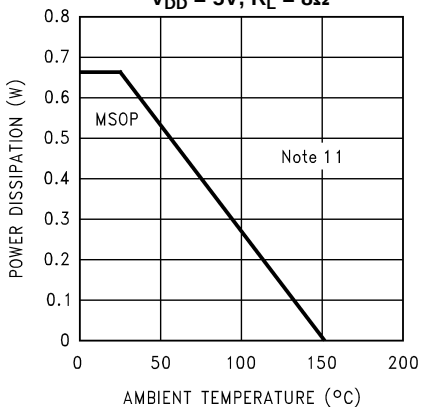

Figure 22.

Power Derating - 8 Bump µSMD P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω

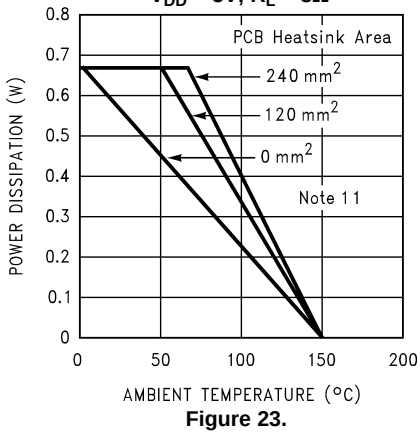

Figure 23.

Power Derating - 9 Bump µSMD P_{DMAX} = 670mW V_{DD} = 5V, R_L = 8Ω

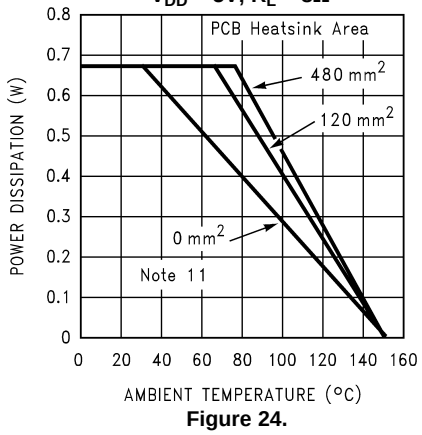

Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Derating - LLP
P_{DMAX} = 670mV
V_{DD} = 5V, R_L = 8

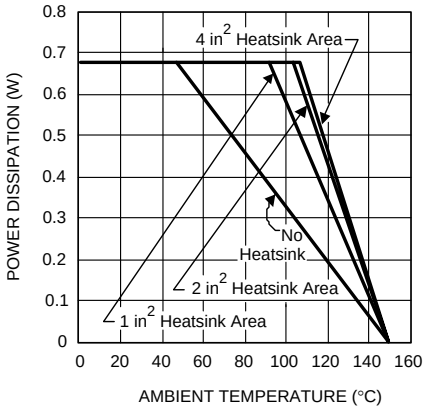

Figure 25.

Output Power vs Supply Voltage

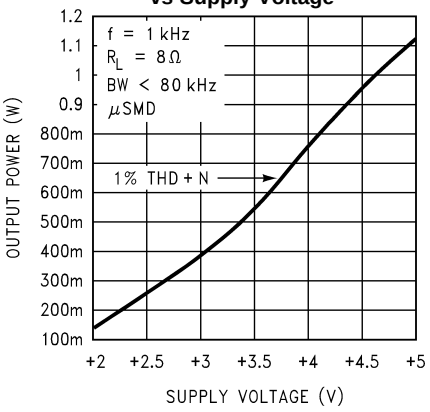

Figure 26.

Output Power vs Supply Voltage

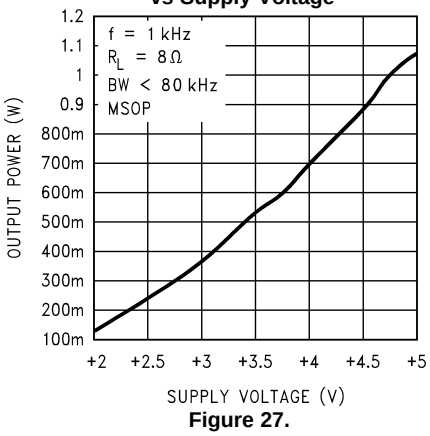

Figure 27.

Output Power vs Load Resistance

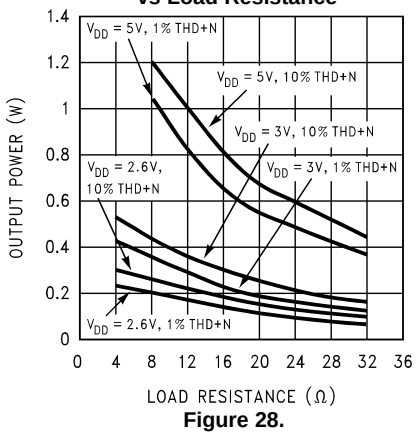

Figure 28.

Clipping (Dropout) Voltage vs Supply Voltage

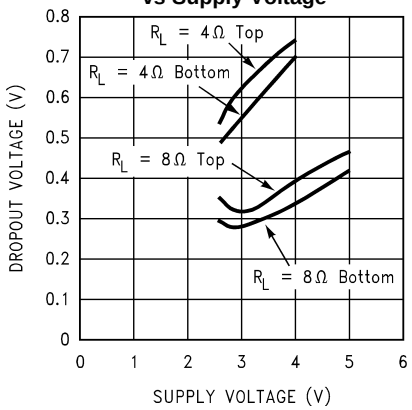

Figure 29.

Supply Current Shutdown Voltage

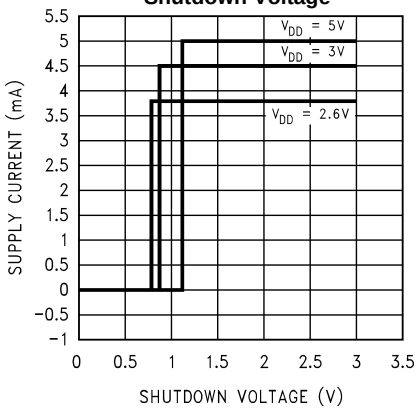

Figure 30.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Shutdown Hysterisis Voltage
V_{DD} = 5V

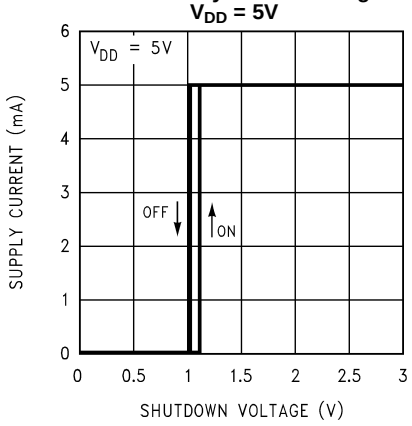

Figure 31.

Shutdown Hysterisis Voltage
V_{DD} = 3V

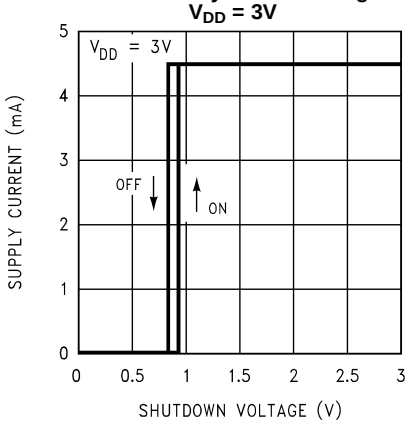

Figure 32.

Shutdown Hysterisis Voltage
V_{DD} = 2.6V

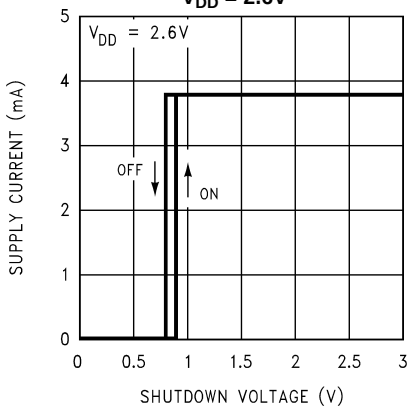

Figure 33.

Open Loop
Frequency Response

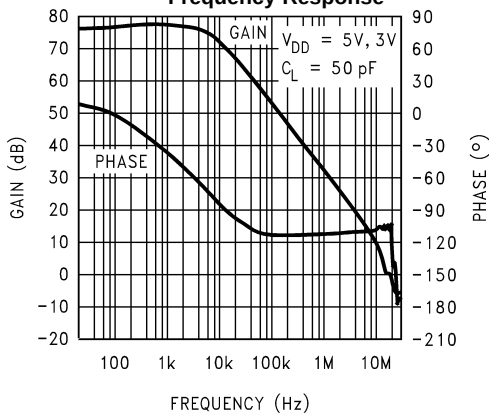

Figure 34.

Frequency Response
vs Input Capacitor Size

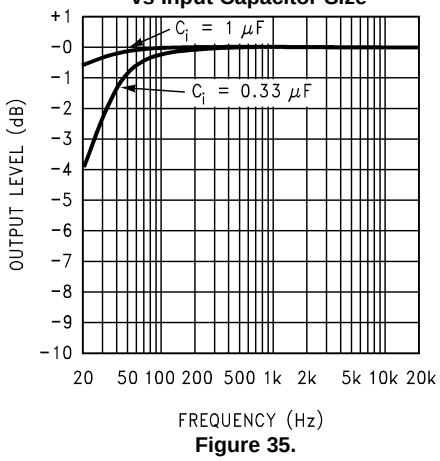

Figure 35.

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APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4879 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20 kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 *(R_f/R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4879, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4879 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from a free air value of 150°C/W, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM4879. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4879 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4879. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

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SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4879 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4879 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.4V_{DC}$, the idle current may be greater than the typical value of 0.1µA. (Idle current is measured with the shutdown pin tied to ground).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground which disables the amplifier. If the switch is open, then the external pull-up resistor to V_{DD} will enable the LM4879. This scheme ensures that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4879 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4879 is unity-gain stable which gives the designer maximum system flexibility. The LM4879 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

SELECTION OF INPUT CAPACITOR SIZE

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4879 turns on. The slower the LM4879's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF is recommended in all but the most cost sensitive designs.

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AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω AUDIO AMPLIFIER

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the TYPICAL PERFORMANCE CHARACTERISTICS section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 3 and add the output voltage. Using this method, the minimum supply voltage would be (V_{opeak} + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the TYPICAL PERFORMANCE CHARACTERISTICS section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{3}$$

5V is a standard voltage, in most applications, chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4879 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{4}$$

$$A_{VD} = (R_f/R_i)\ 2 \tag{5}$$

From Equation 4, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20 kΩ, and with a A_{VD} of 3, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

f_L = 100 Hz/5 = 20 Hz

f_H = 20 kHz * 5 = 100 kHz

As stated in the EXTERNAL COMPONENTS DESCRIPTION section, R_i in conjunction with C_i create a high pass filter.

$C_i \geq 1/(2\pi * 20\ k\Omega * 20\ Hz) = 0.397\ \mu F$; use 0.39 µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100 kHz, the resulting GBWP = 300 kHz which is much smaller than the LM4879 GBWP of 10 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4879 can still be used without running into bandwidth limitations.

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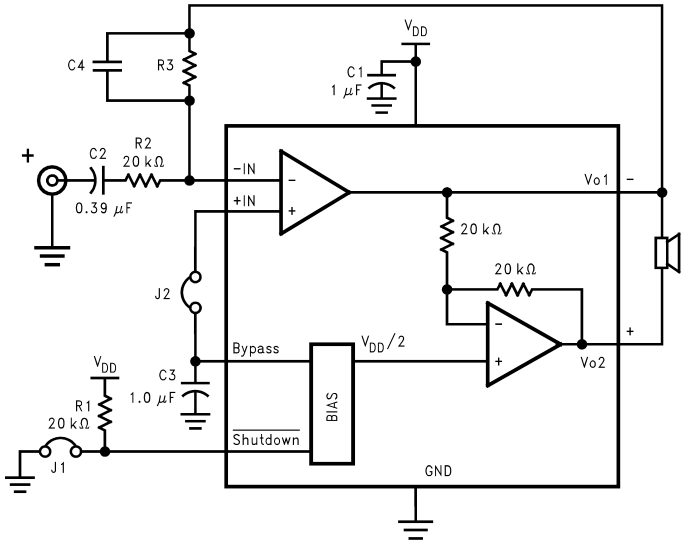

Figure 36. Higher Gain Audio Amplifier

The LM4879 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 36 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

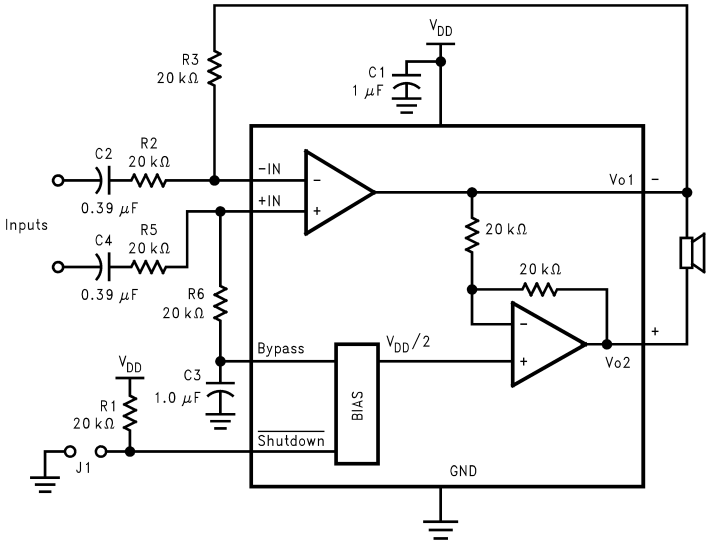

Figure 37. Differential Amplifier Configuration for LM4879

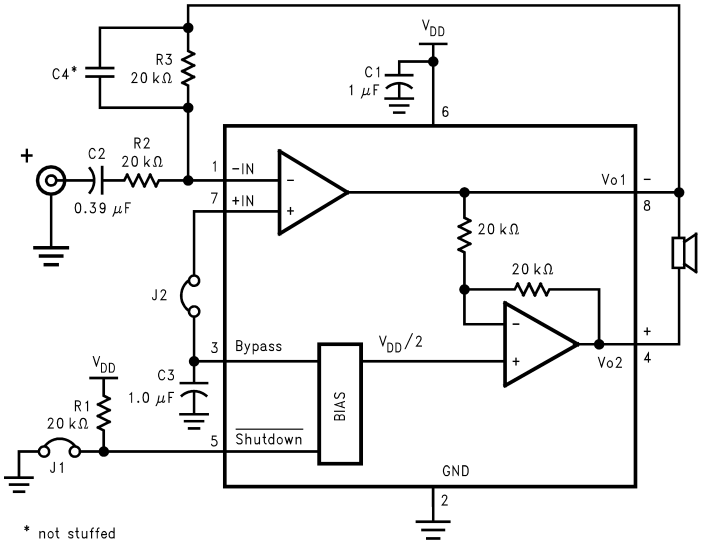

Figure 38. Reference Design Board and Layout - DSBGA

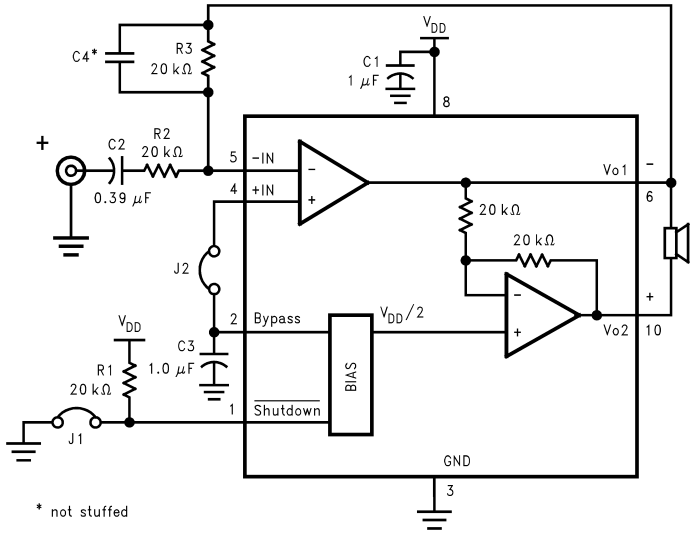

Figure 39. Reference Design Board and PCB Layout Guidelines - VSSOP and SO Boards

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LM4879 DSBGA BOARD ARTWORK

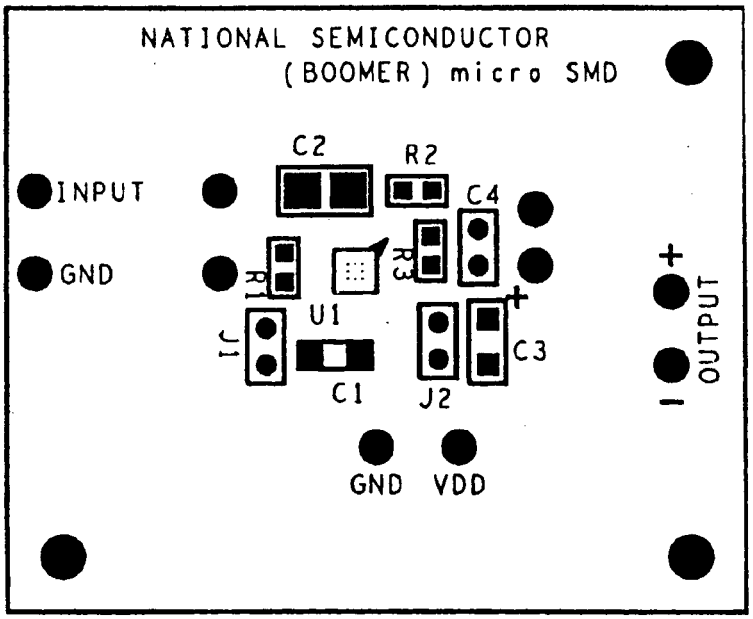

Figure 40. Silk Screen

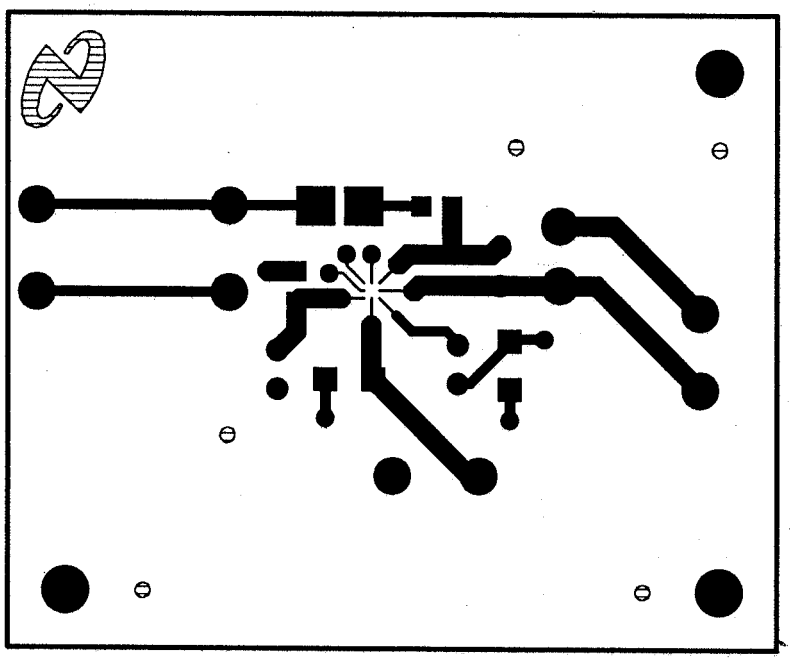

Figure 41. Top Layer

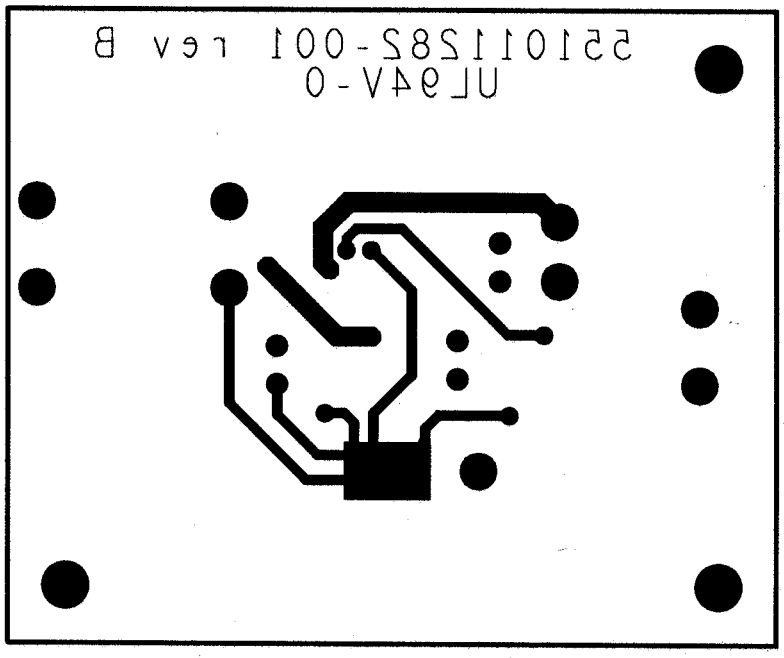

Figure 42. Bottom Layer

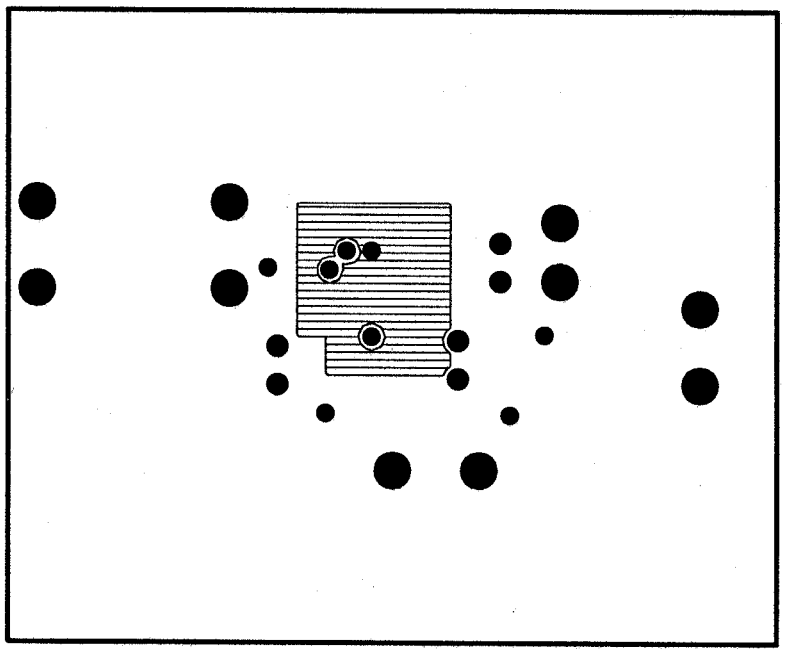

Figure 43. Inner Layer Ground

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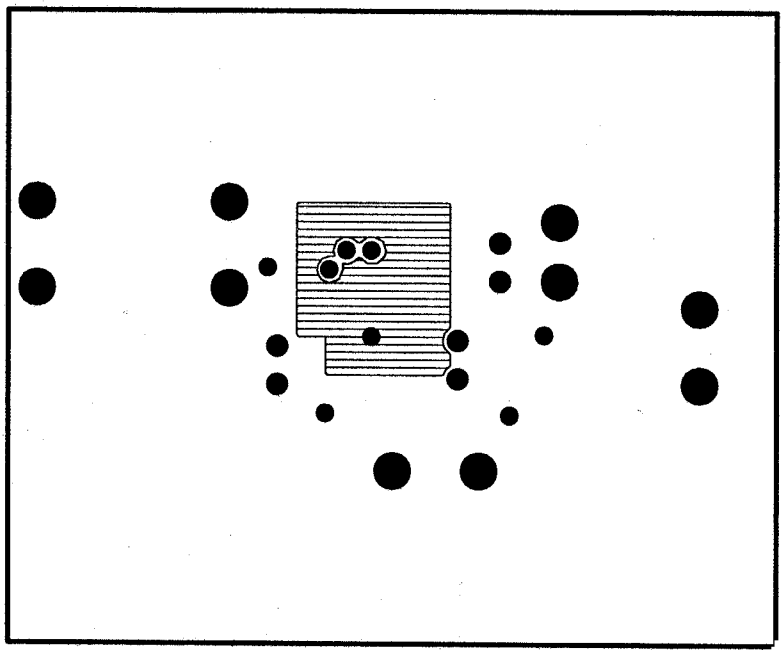

Figure 44. Inner Layer V_{DD}

LM4879 VSSOP DEMO BOARD ARTWORK

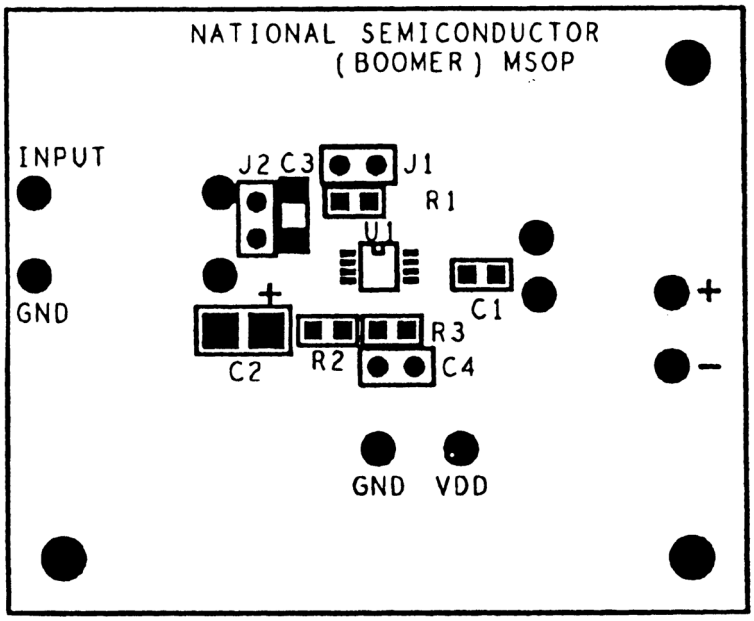

Figure 45. Silk Screen

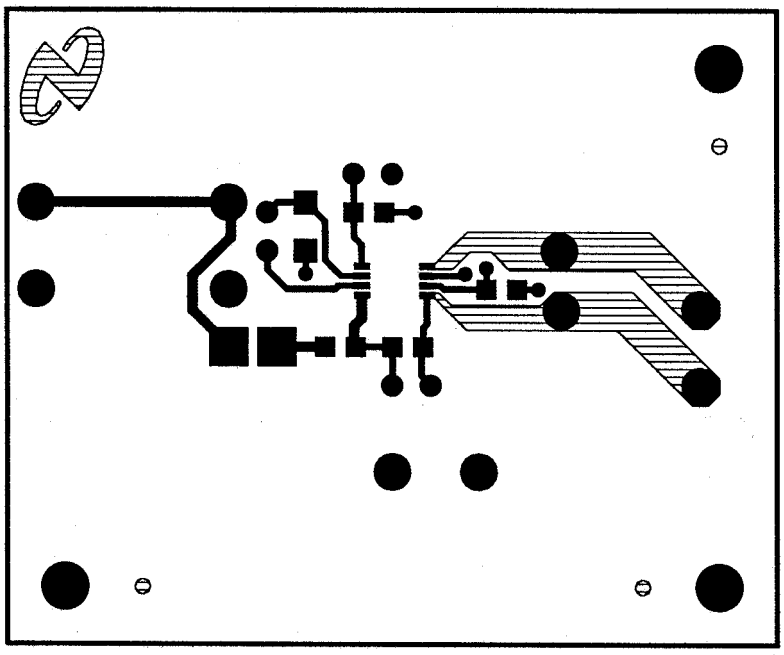

Figure 46. Top Layer

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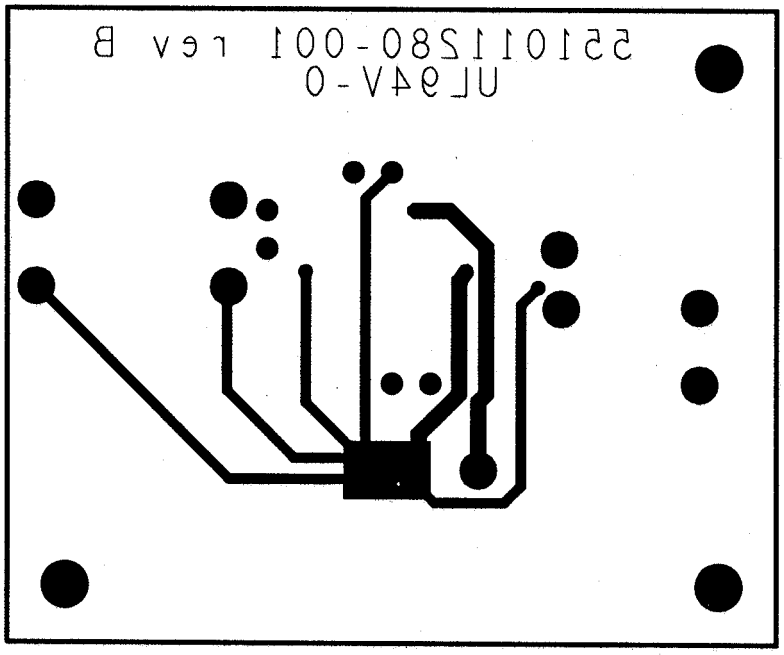

Figure 47. Bottom Layer

Table 1. Mono LM4879 Reference Design Boards Bill of Material for all 3 Demo Boards

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4879 Mono Reference Design Board	1	
10	482911183-001	LM4879 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1.0uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1, R2, R3
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1, J2

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LM4879 WSON DEMO BOARD ARTWORK

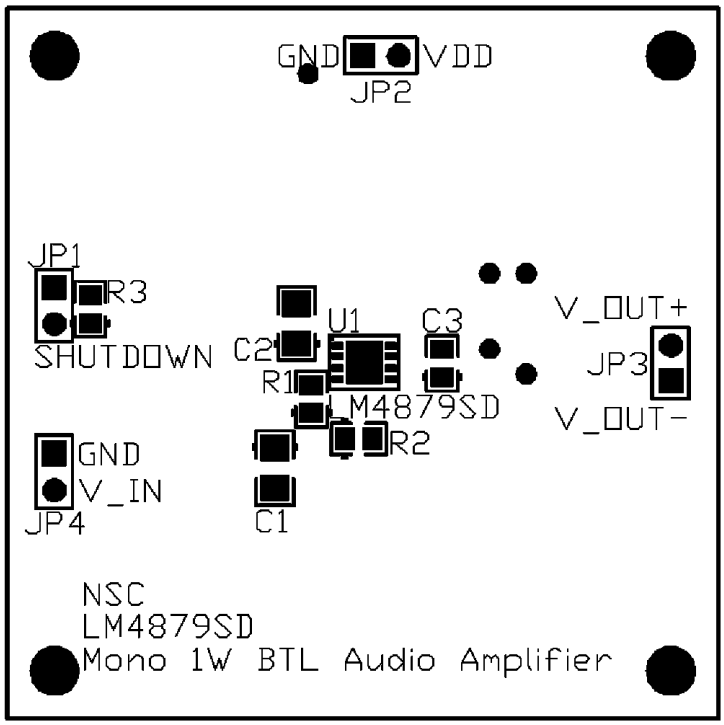

Figure 48. Silk Screen

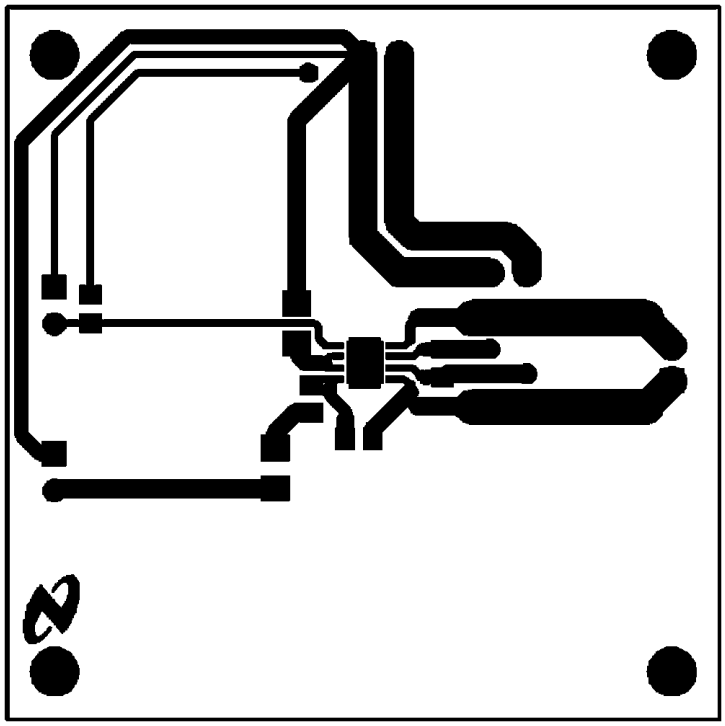

Figure 49. Top Layer

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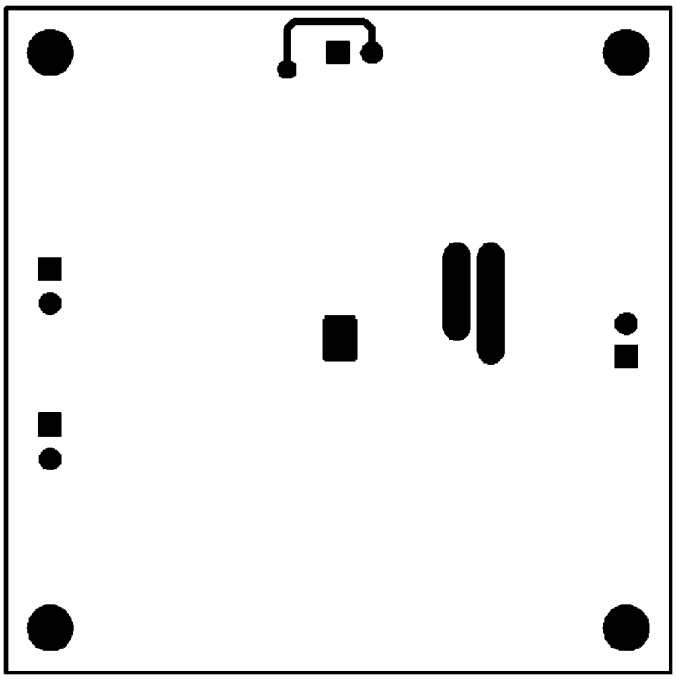

Figure 50. Bottom Layer

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

POWER AND GROUND CIRCUITS

For 2 layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

SINGLE-POINT POWER / GROUND CONNECTIONS

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

PLACEMENT OF DIGITAL AND ANALOG COMPONENTS

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

AVOIDING TYPICAL DESIGN / LAYOUT PROBLEMS

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

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REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4879MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	G79	Samples
LM4879SD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	L4879SD	Samples
LM4879SDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	L4879SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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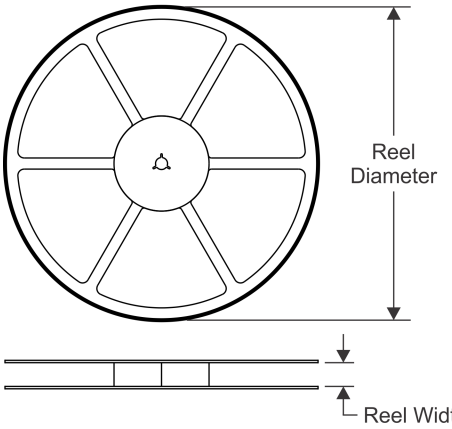
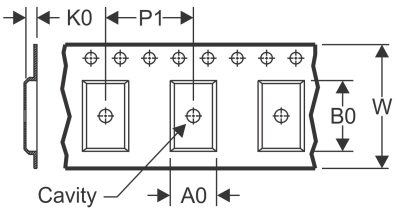
TAPE AND REEL INFORMATION

REEL DIMENSIONS

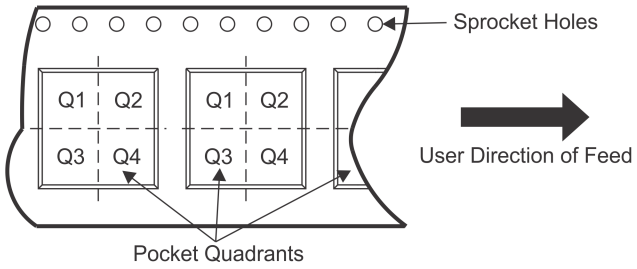


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

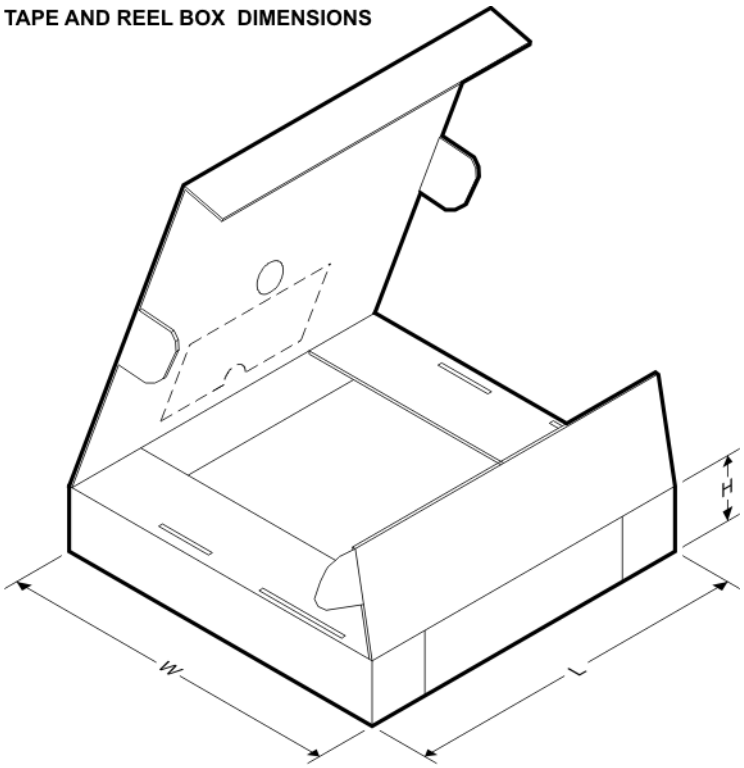
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4879MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4879SD/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM4879SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

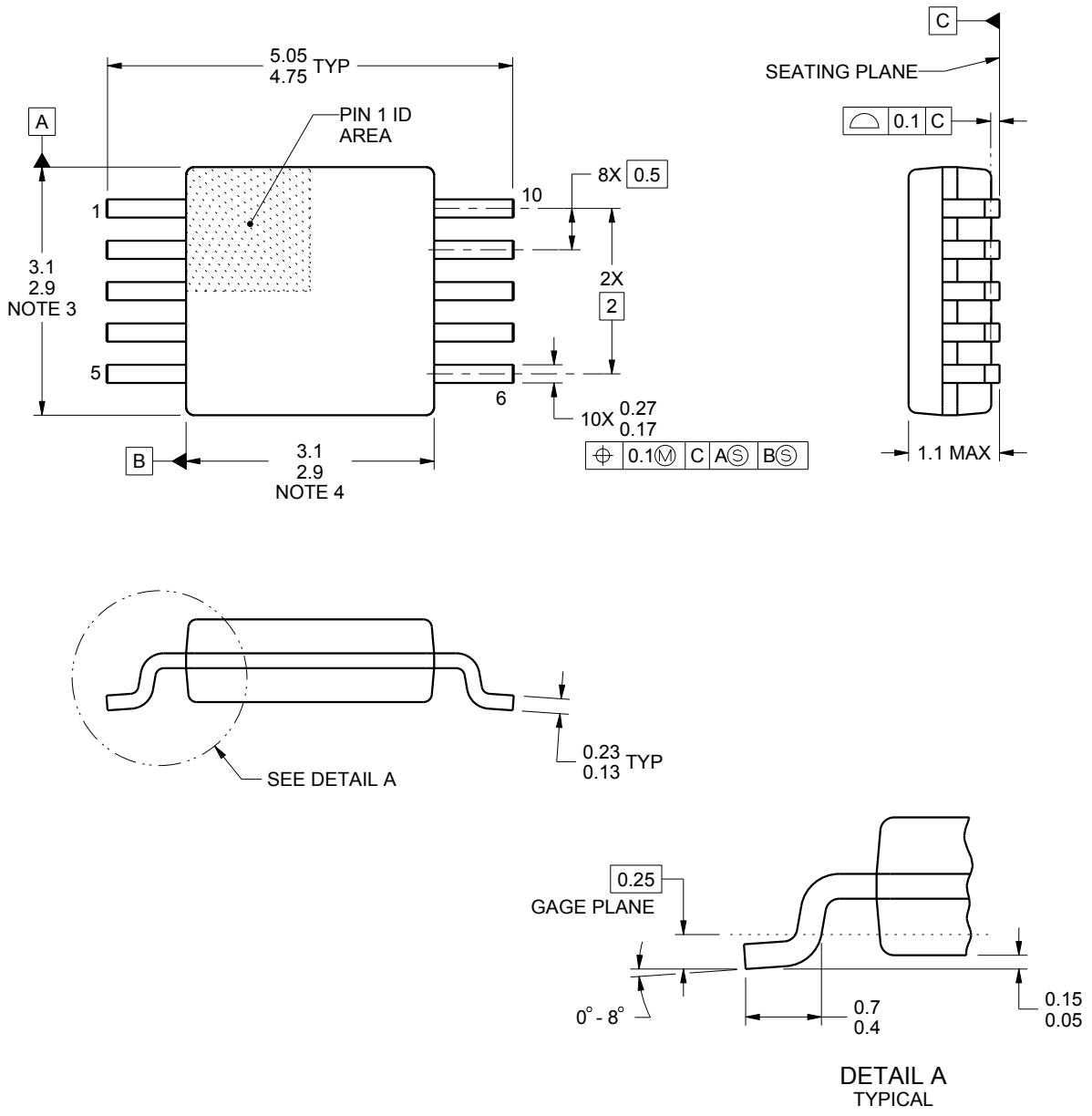
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4879MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM4879SD/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LM4879SDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

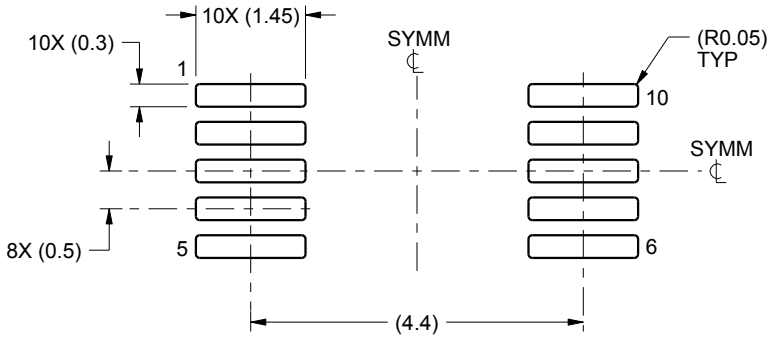
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

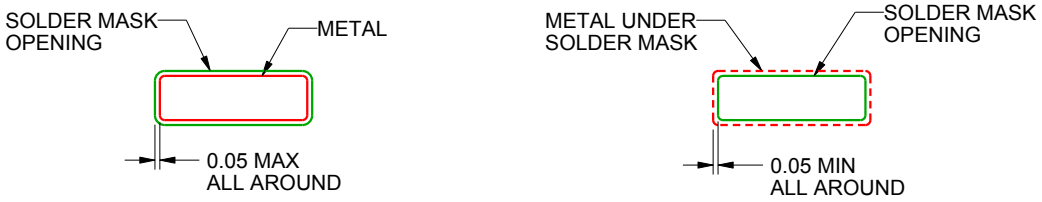


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

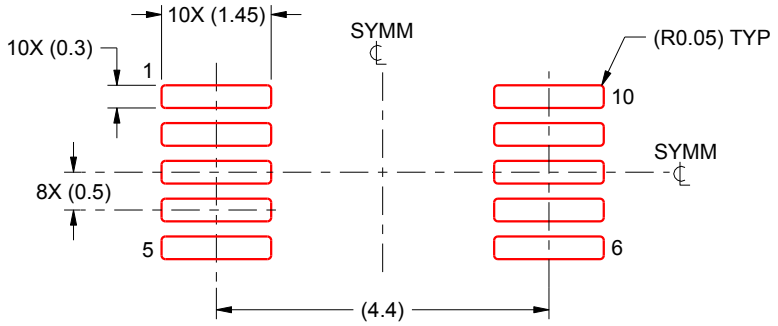


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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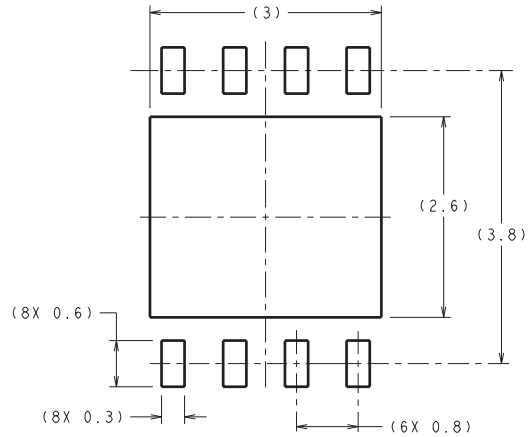
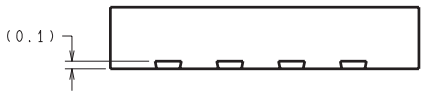
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

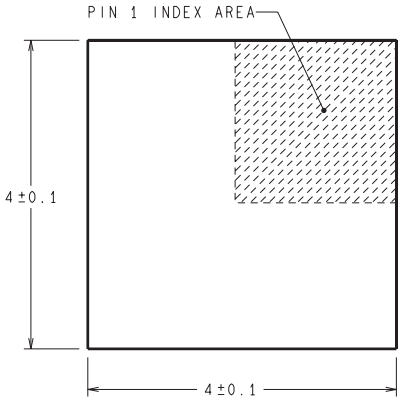
NGT0008A

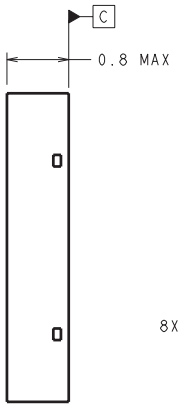


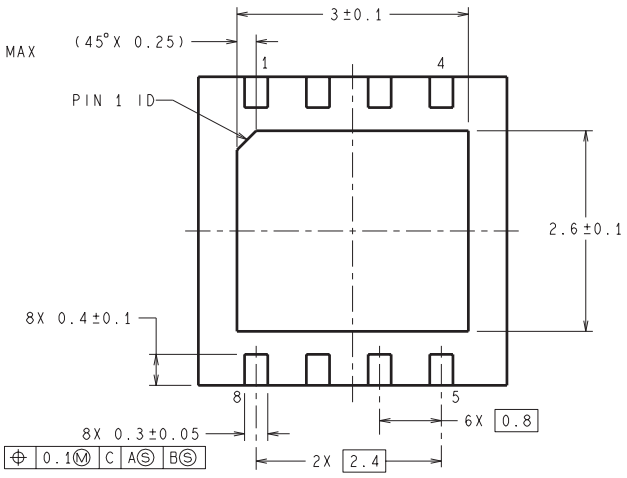
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN







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